SKiiP®

Features

- **SKiiP:** SEMIKRON integrated intelligent Power is a power semiconductor subsystem
- SKiiP integrates power semiconductor switches, heat sink and gate driver unit with protection and monitoring circuit
- SKiiP 3 is the successor product for SKiiP 2 with increased power density and is compatible to SKiiP 2
- Based on SKiiP pressure contact technology which allows a compact power module design with very low thermal resistances, high thermal cycling capability and low parasitic stray inductances
- Equipped with closed loop current sensors, used for short circuit and over-current protection
- Normalized analog voltage signals of the actual AC-current value, the actual ceramic substrate temperature value and the actual DC-link voltage value (optional, depends on type) are available at the DIN41651 gate driver connector of the SKiiP for use in the control unit

Type Designation System

SKiiP ❶ ❷ ❸ ❹ ❺ ❻ ❼ ❽ ❾ ❿

SKiiP 2: SKiiP 3 4 2 G D 12 0 - 3 DU L

SKiiP 3: SKiiP 5 1 3 G D 12 2 - 3 DU L

❶ nominal current I_C (@ $T_{heat\ sink}$ = 25 °C) divided by 100 as e.g. 500 A → 5, can contain 2 letters e.g. 15,

❷ SKiiP 2: chip specification / SKiiP 3: insulation DCB (direct copper bonded) ceramic substrate type

0: aluminum nitride (AlN) DCB ceramic (SKiiP3 only)

1: aluminum oxide (Al_2O_3) DCB ceramic

❸ SKiiP generation , e.g. 3 for 3rd generation

❹ chip type as e.g. G = IGBT

❺ circuit

B: 2 pack (half bridge, dual)

H: 4 pack (single phase bridge)

D: 6 pack (3 phase bridge)

DL: 6 pack + brake chopper

❻ voltage class

12: V_{CES} = 1200 V

17: V_{CES} = 1700 V

❼ chip generation (see table in section IGBT- and Power-MOSFET modules)

❽ number of used modular half bridges (2 packs)

❾ gate driver designator

D: gate driver

DU: gate driver with DC-link voltage measurement and over voltage protection

DUF: gate driver with DC-link voltage measurement, over voltage protection and fiber optical interface (optional for GB type only)

DF: gate driver with fiber optical interface (optional for GB type only)

E/A: brake chopper voltage level for 400V/460V mains voltage (for 1200V-SKiiP GDL only)

❿ heat sink designator

L: standard profile for forced air cooling

W: standard profile for liquid cooling

Please note: Datasheets and type designation of the former SKiiP 2 standard types before 01/04 are at our homepage www.semikron.com under SKiiP, "former data sheets". Further information available on request.

Which SKiiP should I use?

Generally speaking SKiiP 3 is recommended for new designs, especially in applications where a very high power density is required. The table gives a survey of the available types (n.a. <=> not available; I_C given at T_j = 150 °C, T_s = 25 °C).

	6 pack (GD)	**6 pack with brake-chopper (GDL)**	**2 pack (GB)**
SKiiP 2	**I_C [A]**	**I_C [A]**	**I_C [A]**
1200 V	150 - 300	150 - 300	400 - 1200
1700 V	150 - 250	contact SEMIKRON	500 - 1000
SKiiP 3	**I_C [A]**	**I_C [A]**	**I_C [A]**
1200 V	300 - 600	n.a.	1000 - 2400
1700 V	500	n.a.	1000 - 2400

Please note for SKiiP 3 there do exist two types of ceramic substrate, Aluminum Nitrite and Aluminum Oxide. The first one has a very good thermal conductivity which is suitable in water cooled applications, whereas the later one is basically supposed for standard air cooled applications. For SKiiP 2 only Aluminum Oxide is used.

The current values I_{RMS1} and I_{RMS2} of the SKiiP overview table are calculated output currents of a three phase PWM-Inverter with typical operating conditions. Continuous I_{RMS} is limited to 400A per AC-terminal. I_{RMS1} stands for continuous current at following conditions

V_{CES} V	V_{out} V	V_{DC} V	cos	f_{sw} kHz	f_{out} Hz	$T_{j(max)}$ °C	T_a °C
1200	400	650	0,85	5	50	125	40
1700	690	1100	0,85	2	50	125	40

I_{RMS2} stands for a nominal inverter current with 150 % overload capability for 60 s and an output frequency range 2...50 Hz.

For other operating conditions please use our online calculation tool SEMISEL.

Technical Explanations

SKiiP technology

SKiiP technology is the patented technology on which SKiiP modules are based. The main characteristic features of SKiiP technology are

- the base plate free power section
- the spring pressure contact of all thermal and electrical contacts
- the internal low inductive paralleling of inverter legs

SKiiP System power section assembly (Fig. 1, see at the end of this chapter)

The electrical main and auxiliary terminals are not soldered to the insulated ceramic substrate but pressed. The insulated ceramic substrate is pressed to the heat sink. The pressure contacts are responsible for superior thermal cycling capability of SKiiP Systems. In addition they provide simple assembly.

Fig. 2 shows the paralleling of ceramic substrates to achieve high output current capability. This feature of the SKiiP technology provides low stray inductance values in the commutation circuit and therefore allows high utilization of the IGBT blocking voltage V_{ces}.

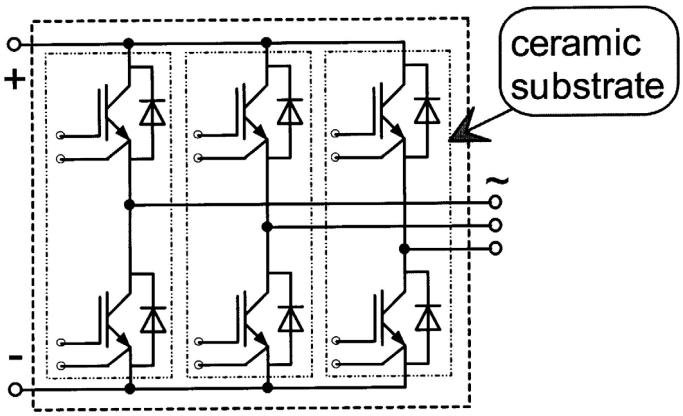


Fig. 2 Paralleling of ceramic substrates

Family of Standard SKiiP Systems

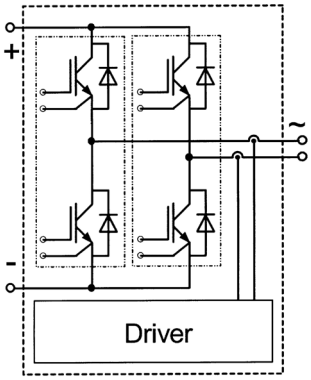


Fig. 3 2-fold SKiiP System

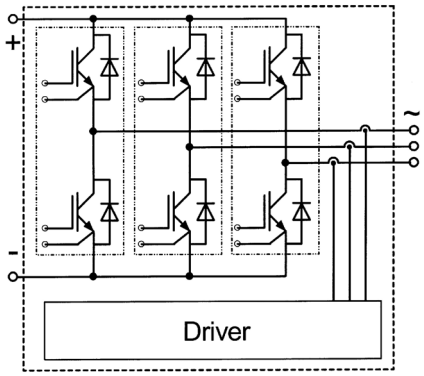


Fig. 4 3-fold SKiiP System

One SKiiP system contains 2, 3 or 4 single ceramic substrates as shown in the block diagrams.

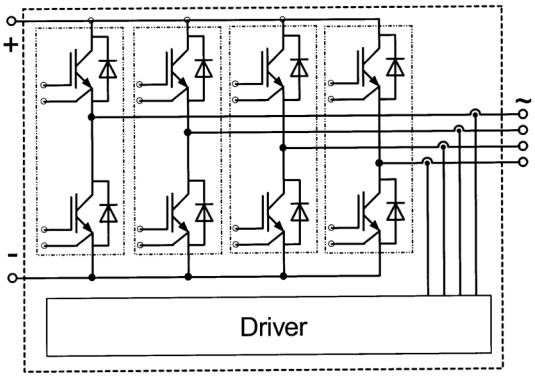


Fig. 5 4-fold SKiiP System

Each ceramic substrate contains a full phase leg with upper (TOP) and lower (BOTTOM) IGBT as well as the corresponding freewheeling diodes. In connetion with the integrated gate driver different power electronic circuits are realised. The following table gives a survey of the available circuits:

circuit	2 substrates (2-fold)	3 substrates (3-fold)	4 substrates (4-fold)
GB	SKiiP 2/3	SKiiP 2/3	SKiiP 2/3
GD		SKiiP 2/3	
GDL			SKiiP 2

Please note: To parallel 2, 3 or 4 power sections of the SKiiP System type the user must parallel the DC and AC terminals to each other. SEMIKRON recommends dedicated bus bars for AC terminal paralleling (please refer to chapter "Accessories").

Properties of the integrated Gate Driver

Fig. 6 shows the functionality of the phase leg (<=>2-pack) gate driver in a block diagram. The 6 pack gate driver incorporates the same functionality per phase. Additionally SKiiP 2 features a ground fault protection. Trip levels of the ground fault protection are given in the corresponding data sheet.

Gate Driver Block Diagram (Fig. 6, see at the end of this chapter)

Insulation

Magnetic transformers are used for insulation between gate driver primary and secondary side. The circuit used for the DC voltage measurement is designed, manufactured and tested according to standard EN50178 (VDE 0160). The SKiiP System insulation test voltage is depending on $V_{CC(max)}$. The individual isolation test voltage level is given in the data sheet. The temperature sensor is insulated on the ceramic substrate.

Please note: The insulation of the temperature signal is a basic insulation only. In a failure case the plasma of an arc can apply high potential to the temperature sensor. Equipment which is designed according to EN50178 must have further insulation for all parts which might be touched by a person.

User Interface - X1

For the individual pin array, please have a look on the seperate interface description.

Please note: Do not remove the plug with applied voltage of the power supply. This can lead to unspecified voltage levels at the output stages of the driver with the risk of destructions.

Digital Input

Figure 7 shows the schematic of the SKiiP 2 and SKiiP 3 digital input lines. A 1 nF capacitor is connected to the input to obtain high noise immunity. This capacitor can cause for current limited line drivers a little delay of few ns, which can be neglected. We recommend choosing the line drivers according to the demanded length of the ribbon cable. It is compulsory to use circuits which switch active to +15 V and 0 V. Pull up and open collector output stages must not be used for TOP/BOT control signals.

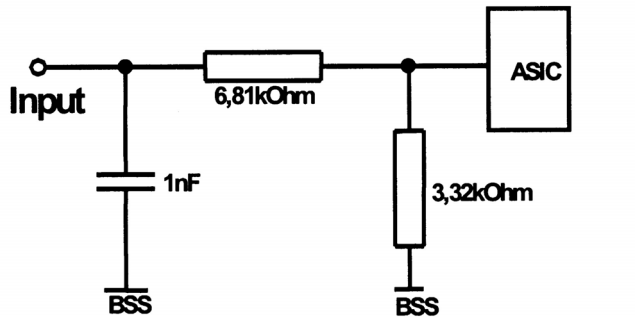


Fig. 7 User Interface - TOP/BOT input

Analog outputs

Figure 8 shows the schematic of the SKiiP 2 and SKiiP 3 analog output lines. The 475 Ω resistor in series with the voltage follower does avoid short circuit damages. Please ensure that the maximum driven current by the output operational amplifier does not exceed 5 mA.

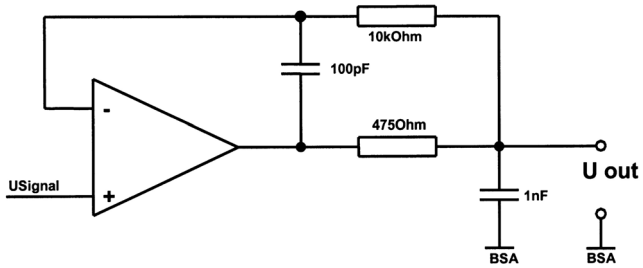


Fig. 8 User Interface- Analog Signal Output

For a trouble-free interaction of SKiiP and user side control it is necessary to adapt the customer input to the SKiiP outputs. For that reason the auxiliary analog signal ground BSA shall be used when analog signals are measured. The ground BSA is on the SKiiP driver board on the same potential as BSS, which is the ground of the power supply. The difference is that the BSA line is not used for supply currents and for that reason no voltage drop due to supply current will be caused.

In the following section a schematic (Fig. 9) and a description is given for an analog input circuit on the controller board of the user.

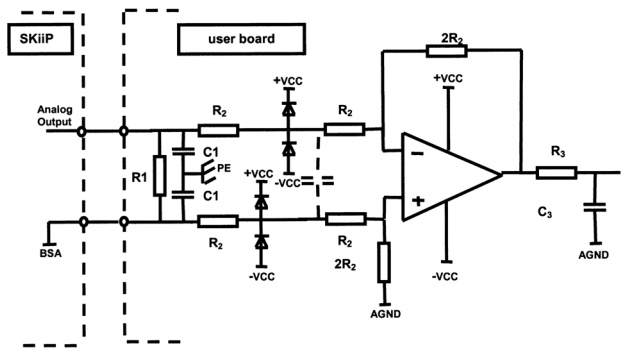


Fig. 9 Symmetric Wired Differential Amplifier

The circuit in Fig. 9 is a symmetrical wired differential amplifier.

- At the input is a 10kΩ resistor (R_1). The interference sensitivity of the over all circuit (user control, driver) is reduced by a continuous current flow through this resistor.
- Capacitor C_1 leaks differential and common mode high-frequency interference currents. This capacitor should not be larger than 100 pF to ensure that there is no additional time delay in the system.
- The symmetrical wiring of the amplifier is as follows. Please note that no capacitor is in parallel to the feedback resistor and also to the resistor of the non-inverting input to ground ($2R_2$). These capacitors have often higher tolerances, so the common-mode rejection of the circuitry is reduced by this effect.
- The input resistor should be split up and installed between the clamping-diodes. The current in the diodes is limited by this resistor. A diode with a low reverse current should be selected e.g. 1N4148.
- If a low pass filtering shall be implemented in the input circuit, this should be done with a capacitor between the input resistors (see dotted lines). In most cases this capacitor is not necessary and the smoothing can be realised by a simple R-C network (R_3, C_3) at the end of the operational amplifier.

Error Latch and Error Feedback

Any error detected will set the error latch and force the output "ERROR OUT" into HIGH state. Switching pulses from the controller will be ignored. Reset of the error latch is only possible with no error present and all input signals in LOW state for the time Tp_{RESET} = 9 µs. All logical error outputs are open collector transistors with $V_{external}$ = 3,3 - 30 V / I_{max} = 15 mA. (Low signal = "no error" - wire break monitoring). We recommend to set the external pull-up voltage as high as possible. An external pull-up resistor $R_{pull-up}$ to the controller logic high level is required. The resistor has to be in the range: $V_{external}/I_{max} < R_{pull-up} < 10\ k\Omega$)

Example:

for $V_{external}$ = 15 V the resistor should be in the range $R_{pull-up}$ = (15 V / 15 mA) - 10 kΩ = 1 kΩ - 10 kΩ

The external filter capacitor C_{ext} is not compulsory but for noise immunity reasons recommended. We advice to choose a value of something in the range of a few nF, because the RC time constant must not exceed the minimum error duration time of 9 µs.

- Fig 10 illuminates the principle of the Error output for SKiiP 2. The error transistor is an ordinary open collector transistor. The resistor R_{sens} acts as sensor for the short circuit protection. In case that the current exceeds the specified I_{max} = 15 mA the transistor will be turned off and the error signal can be detected by the customer. This way the error transistor is short circuit proof.

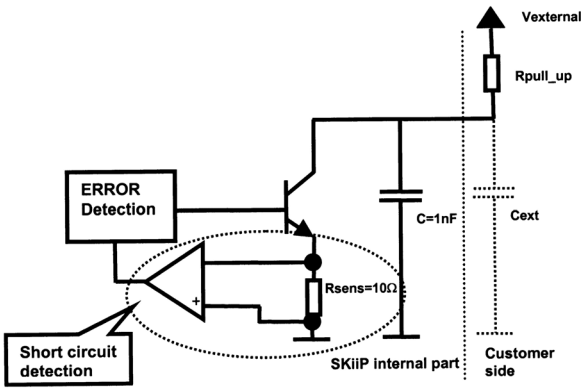


Fig. 10 SKiiP2 - Open Collector Error Transistor

- For SKiiP 3 this circuit is simpler as can be seen in Figure 11.

Please note: The error output of SKiiP 3 is not short circuit proof.

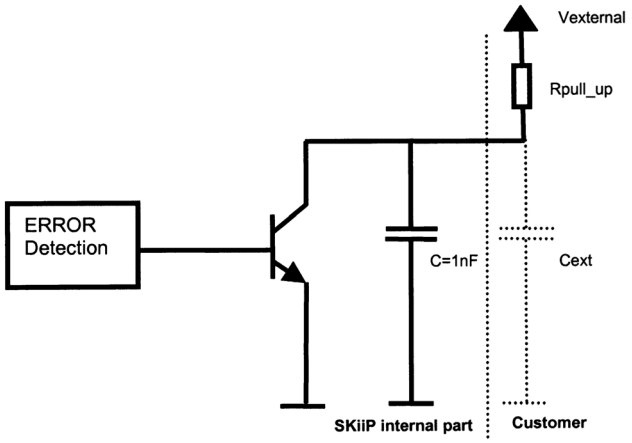


Fig. 11 SKiiP 3 - Open Collector Error Transistor

Requirements of the Auxiliary Power Supply

The table shows the required features of an appropriate power supply for a SKiiP System. All values are related to one SKiiP. In case that the gate driver is supplied with 24 V it is possible to use 15 V provided at the DIN 41651 connector of the gate driver as an auxiliary power supply, e.g. for a level-shifter at the controller's output signals.

	SKiiP 2	SKiiP 3
unregulated 24 V power supply	20 - 30 V	13 - 30 V
regulated power supply 15 V ± 4 %	15 V	please use input of unregulated 24 V power supply
I_{out}15 V (can be used if 24 V supply is active)	<50 mA	<50 mA

minimum peak current of auxilary 15 V supply	1,5 A	-
minimum peak current of auxiliary 24 V supply	1,5 A	1,5 A
max. rise time of auxiliary 15 V supply (the voltage slope has to be continuous - no plateau in voltage slope)	50 ms	-
max. rise time of auxiliary 24 V supply (the voltage slope has to be continuous - no plateau in voltage slope)	50 ms	<2 s
power on reset completed after	130 ms	150 ms

Please note: Do not apply switching signals during power on reset.

The current consumption of SKiiP Systems depends on the level of supply voltage used, the standby current of the gate driver, the switching frequency, the capacitance of the IGBT gates in use and on the actual main AC-current. In the data sheets for each gate driver an equation is given which describes the current consumption depending on standby current, switching frequency and AC output current. Please rate the power supply that way, that the continuous current is at least 20 % higher that the calculated consumption current from the SKiiP. The rated peak current of the supply must fulfill the specification in the table.

Since SKiiP 3 uses a switched amplifier for the compensated current sensor the current consumption of SKiiP 3 has been reduced towards SKiiP 2.

In the datasheets the equation for the evaluation of the current consumption is given assuming supply with 24 V. Additionally the SKiiP 2 datasheets provide an equation to calculate supply current for operation with 15 V.

Example for SKiiP 2 (SKiiP 1242GB120-4D @ 24 V):

I_{S2} = 340 mA + 490 mA * f_s/f_{smax} + 3,5 mA * I_{AC} / A

Example for SKiiP 3 (SKiiP 2403GB122-4D @ 24 V):

I_{S2} = 280 mA + 460 mA * f_s/kHz + 0,0003 mA *$(I_{AC}/A)^2$

Please note: The switch mode amplifier of SKiiP 3 compensated current sensor causes a quadratic relationship to AC current level.

Maximum switching frequency $f_{sw(max)}$

The maximum switching frequency of the SKiiP is limited by the average current of the driver power supply and the power dissipation of driver components. The given value for fsw(max) in each individual data sheet is valid for an ambient temperature of 25 °C, for higher temperatures a reduction of fsw for SKiiP 3 might be necessary. (see fig. 12)

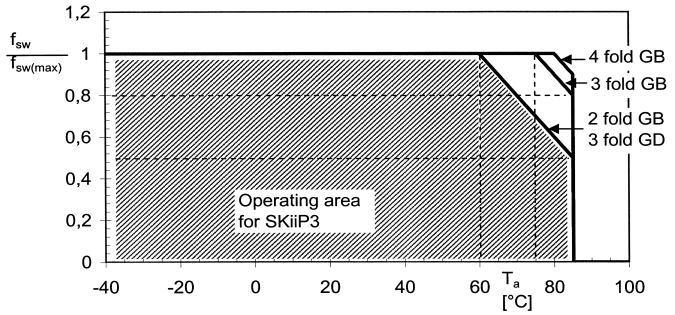


Fig. 12 Maximum switching frequency for SKiiP 3 as a function of the ambient temperature

Protection and supervisory functions

SKiiP 2/3 gate drivers feature the following protection and supervisory functions

- Interlock and dead time generation for TOP and BOTTOM IGBT
- Short pulse suppression
- Input pulse shaping
- Input signal clamping
- Under voltage monitoring of the (internal) supply voltage on primary side
- Transient over voltage and inverted polarity protection by suppressor diode
- Over temperature protection (if forced air cooling is used)
- Short circuit and over current protection (by current sensor and V_{cesat} monitoring)
- Line to ground fault protection (only for type SKiiP 2 GD)
- Over voltage protection of the DC link voltage (optional; for SKiiP 3 GD as standard)

The following chapter gives a description of the SKiiP System protection and supervisory functions as illustrated in the block diagram. The datasheets include timing and trip level data.

OCP - (O)ver (C)urrent (P)rotection and Short Circuit Protection

As shown in the block diagram SKiiP Systems feature integrated current sensors per AC terminal. These current sensors can be used for AC current control. In addition they are used to protect the SKiiP System against over currents. The over current protection reacts independently of the temperature level and provides a reliable protection of the SKiiP System. If the AC output durrent is higher than the maximum permissible level of 125 % I_C (exception: SKiiP 3 with AIN ceramic substrate), the IGBTs are immediately switched off and switching pulses from the controller are ignored. The error latch is set. The output "ERROR

OUT" is in HIGH state. In addition a V_{CEsat} monitoring circuit is implemented to protect the phase leg against internal short circuit („shoot through protection).

Over temperature protection

The temperature of the ceramic substrate is monitored by an integrated temperature sensor. The over temperature trip threshold has been chosen at T = 115 ± 5 °C. At that temperature the IGBTs are switched off and switching pulses from the controller are ignored. The error latch is set. The outputs "Overtemp. OUT" and "ERROR OUT" are in HIGH state.

Please note: the output "ERROR OUT" is an open collector output which needs an external pull up resistor.

The over temperature trip threshold has been chosen at 115 °C. For most air cooled applications this is sufficient to protect the system. But for water cooled systems or short time overloads the threshold might be too high. In this case there is a need for another protection trip level for what the user can evaluate the analog temperature output to protect the system.

Under Voltage Protection of the Supply Voltage

The under voltage protection of the primary side monitors the internal 15 V DC which is provided by the internal DC-DC converter (converts the unregulated input voltage to 15 V DC) or by controlled + 15 V DC input (SKiiP 2 only). If the under voltage trip level is reached, the IGBTs are switched off and switching pulses from the controller are ignored. The error latch is set. The output "ERROR OUT" is in HIGH state. The table below gives an overview of the trip levels.

under voltage trip level @ condition	**SKiiP 2**	**SKiiP 3**
primary side, supply via 24 V pins	18,5 V	no trip level
primary side, supply via 15 V pins	13,9 V	-
internal regulated + 15 V	13,9 V	13,9 V
internal regulated - 15 V	- 13,9 V	- 13,9 V
secondary side	-	10 V

DC link over voltage protection

This protection is implemented for GD types and optional for GB type SKiiPs.

If the operating DC link voltage is higher than V_{CCmax} the IGBTs are turned off and switching pulses from the controller are ignored. The error latch is set. The output "ERROR OUT" is in HIGH state. The trip level is given in the datasheet.

Short Pulse Suppression

This circuit suppresses short turn-on and off-pulses. This way the IGBTs are protected against spurious noise as they can occur due to bursts on the signal lines. Pulses shorter than 625 ns are for 100 % probability suppressed and all pulses longer than 750 ns get through for 100 % probability. Pulses with a length in-between 625 ns and 750 ns can be either suppressed or get through.

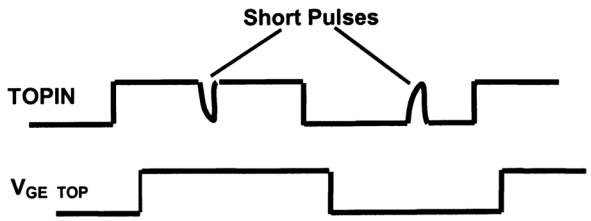


Fig. 13 Pulse Pattern - Short Pulse Suppression

Dead Time Generation ("TOP/BOTTOM interlock")

The interlock circuit prevents that the TOP and the BOT IGBT of one half bridge are switched on at the same time (internal short circuit). The internal interlock time is adapted to the power semiconductors, i.e. it is chosen as small as possible to allow high duty cycle but guarantees a safety margin against shoot through losses due to tail currents. The dead time does not add to a dead time given by the controller. Thus the total dead time is the maximum from either „built in dead time“ or „controller dead time“. Please note that the propagation delay of the driver is the sum of interlock dead time (t_{TD}) and driver Input output signal propagation delay of the driver ($t_{d(on/off)IO}$) as shown in figure 13. The I/O-delay ($t_{d(on/off)IO}$) include the time for short circuit suppression. The interlock time is only active in case that the opposite device is switching with an inverted pulse pattern. Moreover the switching time of the IGBT chip has to be taken into account (not shown in figure 13).

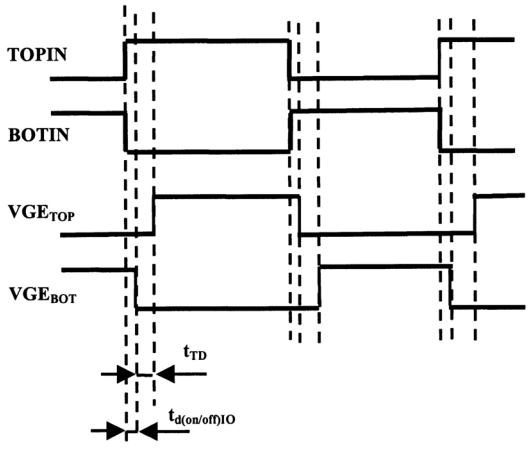


Fig. 14 Pulse Patter - dead time generation

In general, it can be said, that in case both channel inputs (TOPIN and BOTIN) are at high level, the driver outputs (V_{GETOP} and V_{GEBOT} will be turned off, but no error signal will be generated. Short pulses on the complementary

input will be also ignored in the case for any pulses shorter than the short pulse suppression (650 ns).

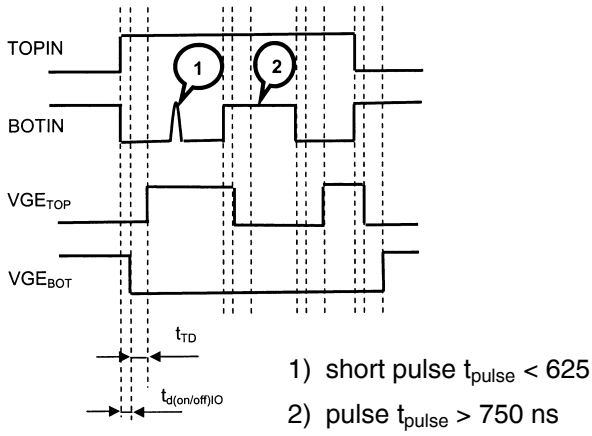


Fig. 15 Signal Logic behaviour for both input pulses in ON state

Error Management

The error management of SKiiP can be described by the following table. Any error condition will cause the error signals on the corresponding pins to go high on the open collector output (indicated by "X").

Error Management of GB-Types

	Pin 3 ERROR HB1 OUT	Pin 5 Overtemp. OUT
V_{CE}-protection HB1	X	
OCP* HB1	X	
temperature protection	X	X
DC-link over voltage protection	X	
Internal supply voltages error	X	

* OPC = Over Current Protection

Error Management of GD-Types

	Pin 3 ERROR HB1 OUT	Pin 6 ERROR HB2 OUT	Pin 9 ERROR HB3 OUT	Pin 11 Over-temp. OUT
V_{CE}-protection HB1	X			
V_{CE}-protection HB2		X		
V_{CE}-protection HB3			X	
OCP HB1	X	X	X	
OCP HB2	X	X	X	
OCP HB3	X	X	X	
temperature protection	X	X	X	X
DC-link over voltage protection	X	X	X	
Ground Fault (SKiiP2 only)	X	X	X	
Internal supply voltage Error	X	X	X	

Integrated Sensor Functions

The SKiiP features the following integrated sensors

- compensated current sensor per pharse leg
- temperature sensor on ceramic substrate
- sensing of DC link voltage (optional)

Integrated Current Sensor

SKiiP integrates one current transformer per power section to measure the AC output current. The measured current is normalized to a corresponding voltage at the DIN 41651 connector. The over current trip level is set to 10 V.

In all SKiiP 2 and SKiiP 3 with aluminum oxide (Al_2O_3) ceramic substrate 100 % of the rated DC current I_C corresponds to 8 V and the over current trip level I_{TRIPSC} is set to 125 % I_C, equivalent to 10 V.

SKiiP 3 systems with aluminum nitride (AlN) ceramic substrate are from an electrical point of view similar to the same sized Al_2O_3 substrate based systems but have a better thermal conductivity and therefore a higher rated DC-current. There is no difference of the driver board (as e.g. current normalization, over current trip level etc.). For that reason both systems have the same relation between the absolute values of current and corresponding voltage. Only the relation in percent to I_C is different. Please refer to the individual datasheets for the corresponding values.

Current transformers are working according to the compensation principle. The magnetic field caused by the load current is detected by a magnetic field sensor. This is not a Hall element but a small coil with a high permeable core. Due to the properties of this sensing element there is no offset failure and almost no temperature dependence. An electronic circuit is evaluating the value of the field sensor and is feeding a current into the compensation coil thus keeping the effective magnetic field to zero. The compensation current gives an image of the load current and is evaluated across a burden resistor with an electronic circuit.

Figure 16 illuminates the compensation principle with the SKiiP 3 current sensor. The SKiiP 3 current sensor uses a switch mode controller for the compensation current versus a linear controller used in the SKiiP 2 current sensor. This leads to remarkably reduced current consumption of the SKiiP 3 current sensor.

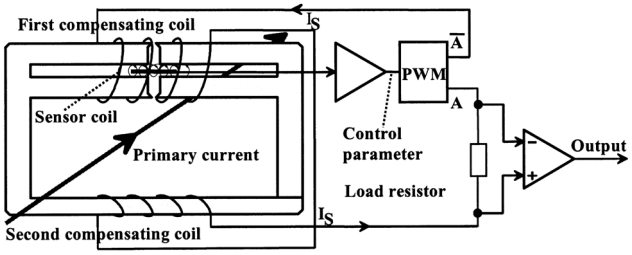


Fig. 16 SKiiP 3 compensated current sensor

The table below compares the data of SKiiP current sensors (one sensor per power section).

parameter	SKiiP 2	SKiiP 3
continuous output current per current sensor	200 A_{rms}	400 A_{rms}
continuous output current, 2 s per current sensor	250 A_{rms}	500 A_{rms}
peak current, 10 µs	3000 A	3000 A
small signal bandwith (- 3 dB)	DC...100 kHz	DC...50 kHz
large signal frequency	DC...1 kHz	DC...1 kHz
response time	< 1 µs	< 1 µs
parasitic capacitance prim. - sec.	40 pF	30 pF

The accuracy of the current sensor depends on several points as there are:

- tolerance of current sensor electronic
- tolerance of burden resistor of current sensor
- tolerance of SKiiP internal amplification circuitry (e.g. by offset of operational amplifiers, tolerances of external passive components etc.)
- tolerance due to temperature drift

The maximum tolerance values can be calculated by the values given in the following equation:

$\Delta I = I_C * k_{Io} + I_{actual} (k_{Ierror} - k_{Io} + |\Delta T| * TC_{Error})$

Parameter	SKiiP 2	SKiiP 3
Offset K_{Io}	0,35 %	0,13 %
Gain Error K_{Ierror}	1,50 %	1,50 %
Temperature Coefficient TC_{Error}	0,001 %/K	0,002 %/K

I_C is the Nominal current per DCB

ΔI is the absolute deviation per DCB

Example:

For a SKiiP 3 (e.g. 513GD172 with I_C = 500 A) is the deviation at the current level of I_{actual} = 300 A and T = 85 °C:

Deviation = 500 A * 0,13 % + 300 A * (1,5 % - 0,13 % + | 85 °C - 25 °C | * 0,002 % / K) = **4,76 A**

Please note that the absolute deviation is given in relationship to the current per DCB. In case that a 2-fold GB is used the deviation is the same compared to a GD type SKiiP for the same current per DCB.

Integrated Temperature Sensor

The integrated temperature sensor is a semiconductor resistor with a linear proportional characteristic to the temperature (PTC characteristic). The sensor is soldered onto the ceramic substrate close to the IGBT and freewheeling diodes and indicates the actual substrate temperature. The sensor is insulated. An evaluation circuit realized on the integrated driver provides a normalized, analog voltage signal of the actual ceramic substrate temperature value (see Fig. 17). The ceramic substrate temperature is very close to the heat sink temperature.

The accuracy of the temperature sensor is approximately ± 3 °C (see also Fig. 15). Please note that the temperature sensor is designed for T_r > 30 °C. The tolerance band is very wide temperatures below 30 °C.

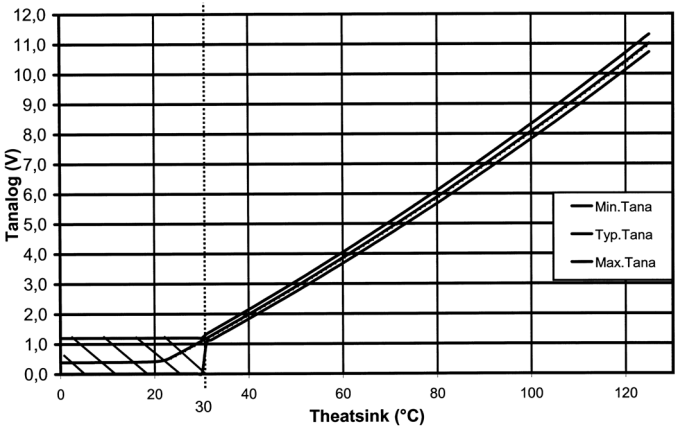


Fig. 17 Analog temperature signal $U_{analog\ OUT}$ vs. T_{sensor}: (at pin "Temp. analog OUT")

Integrated DC link Voltage Monitoring

With the option U "analog DC-link voltage-sense", a normalized, analog voltage signal of the actual DC-link voltage level is available at the DIN 41651 connector of the gate driver. The measurement is realized by a high impedance differential amplifier. The circuit is designed, manufactured and tested according to standard EN50178 (VDE 0160).

Normalization of the actual DC-link-voltage signal and input impedances of the measurement circuit is shown in the table below.

	SKiiP 2 / SKiiP 3	SKiiP 2 / SKiiP 3	SKiiP 2 / SKiiP 3
V_{CES}	$V_{DC} \Leftrightarrow V_{DCanalog}$	Input Impedance	$V_{CCmax} \Leftrightarrow V_{DC-Tripmin}$
1200 V	900 V ⇔ 9 V	5 MΩ	900 V
1700 V	1200 V ⇔ 9 V	6,5 MΩ	1200 V

The failure of the measured signal is ± 2 % @ T_a = 25 °C. The over voltage trip level is V_{ccmax}. The analog output signal $V_{DCanalogOUT}$ is filtered with a time constant of t = 500 µs.

Brake Chopper Driver used in SKiiP 2 type "GDL"

Block diagram brake chopper driver (Fig. 18, see at the end of this chapter)

SKiiP 2 GDL type incorporates a 6-pack (GD) and a brake chopper. The brake chopper of the GDL SKiiP 2 is located at the right side assuming the DC terminals on the bottom. The following paragraphs explain the functionality of the brake chopper driver according to the block diagram Fig. 18:

Internal Control

The bang-bang controller generates the ON and OFF signals for the brake chopper depending on the DC link voltage level. Once the hysteresis comparator is triggered, the minimum ON time for a discharging pulse is typ. 30 µs.

Two standard versions for 1200 V SKiiP 2 are available.

Type	Version E (for U_{line} = 400 V_{AC})	Version a (for U_{line} = 460 V_{AC})
UZ_{max}	730 V	860 V
U_{Zon} (Chopper On)	681 V	802 V
U_{Zoff} (Chopper Off)	667 V	786 V

External Control

The input signal *CHOPPER* ext. ON (PIN 2) can be used for external switching (for example for discharging the DC-link capacitor while having a service). External ON switching is only possible, if the chopper's error latch is not set and does not depend on the actual value of the DC link voltage. The max. switching frequency should not exceed 5 kHz. As designed for open collector drive, this input is not depending on a certain controller logic level. Active LOW from the controller means CHOPPER = ON

Protection

- The IGBT is protected against short circuit by V_{CE} - monitoring.
- Heat sink temperature monitoring. The driver turns off at T = 115°C and the error memory is set.
- DC-voltage monitoring: If the DC voltage exceeds UZmax the driver turns off and the error memory is set.

The chopper driver is protected against over voltage of the 15 V supply by a suppressor diode. This suppressor diode will be destroyed in case of reverse polarity of 15 V supply. The driver is protected against reverse polarity of 24 V power supply.

Error Memory

The error memory is set by various error signals. Switching ON the chopper IGBT is only possible if the error memory is in NO ERROR state. Once the error latch is set, it will remain in ERROR condition until no more error is present and input RESET (PIN 4) is active LOW for min. $t_{pdRESET}$ > 300 ms. After start up of power supply a power on reset takes place.

Error conditions:

a) under voltage condition of the supply voltage
limit value when using 15 V_{DC} (± 4 %): < 13,5 V
limit value when using 24 V_{DC} (20 ... 30 V): < 16 V

b) short circuit (V_{CE} monitoring) of brake IGBT

c) DC-link over voltage: Uz > Uz_{max}

d) Over temperature: T_{chip} > 115 °C ± 5 °C

Error output

Setting of the error latch will create an error signal at the ERROR OUT (PIN 3). This output has an open collector transistor which is optically controlled. An external pull up resistor (max. 30 V / 2,5 mA) must be connected on the controller board to logic HIGH level. Active LOW at driver output means NO ERROR.

Power supply

The driver may be supplied either with 24 V_{DC} (20 ...30 V) or with regulated +15 V_{DC} ± 4 %. If 24 V supply is used 15 V supply must not be used and vice versa.

DC / DC converter

The DC/DC converter provides an isolated power supply with low coupling capacity for the gate drive and its logic. An active LOW input at RESET (PIN 4) from the controller blocks the power supply for the secondary side.

Features of Standard Heat Sinks

SKiiPs are equipped with high performance heat sinks. The data sheets contain transient thermal data referenced to the built-in temperature sensor. This allows the calculation of junction temperature if the generated losses are known. The given thermal resistances represent worst case values.

Evaluation of thermal impedance:

junction sensor (subscript for sensor: "r"):

$Z_{th(j-r)} = \sum R_{th(j-r)n} * [(1 - e^{- t / tau\ n})]$, n = 1,2,3..

sensor ambient:

$Z_{th(r-a)} = \sum R_{th(r-a)n} * [(1 - e^{- t / tau\ n})]$, n = 1,2,3..

To simplify the comparison with other power semiconductor modules SKiiP 3 data sheets also contain the thermal resistance between chip junction and heat sink (subscript for heat sink: "$_s$"). These values are given as typical values.

Please note: The reference point for heat sink temperature (subscript "s") is directly below the hottest chip → the temperature of the reference point is not available in the application environment.

All technical data of SKiiP are incorporated into the SEMISEL simulation software which has online access under http://www.semikron.com

For further explanations of the thermal modeling please read the SEMIKRON application hand book (also available under http://www.semikron.com).

Standard Heat Sink for forced Air Cooling

The drawings are available in the datasheet section. The coefficients of the transient thermal impedance are given in the data sheet (SKiiP 3 only; SKiiP 2 transient thermal impedances are available in a separate document). The given air volumes are valid when the SEMIKRON standard fan SKF16B is used. Please note: Strictly speaking the given transient thermal impedance ($Z_{th(j-r)}$) data are valid together with the SEMIKRON standard heat sink only. They might be adapted for other forced air cooled heat sinks which have a minimum root thickness of 14 mm.

Standard Heat Sink for Liquid Cooling

The drawings are available in the datasheet section. The coefficients of the transient thermal impedance are given in the data sheet. (SKiiP 3 only; SKiiP 2 transient thermal impedances are available in a separate document).

Please note: The given transient thermal impedance ($Z_{th(j-r)}$) data are valid together with the SEMIKRON standard heat sink only and for 50 % / 50 % water glycol cooling liquid. The usage of these value for other liquid cooled heat sinks might cause severe deviations in calculation of thermal resistance.

Options

U-option: DC-link Voltage Sense Monitoring

If a 2 pack SKiiP ("GB" type) is used with U-option the analog voltage signal of the actual DC-link value is present at Pin 12 of the driver interface instead of the signal for the actual heat sink temperature. The 6 pack SKiiP ("GD" type) has DC bus bar voltage and temperature information in the standard version available.

F-option: Connection to the SKiiP System using Fiber optic Interface

With the ,,option - F" switching and error signals are transferred via fiber optic connectors. The fiber optic adapter (Fig. 19) is fixed at the cover of the SKiiP System, and connected to the integrated driver via a short flat cable. Fiber optic connectors from Hewlett Packard's HFBR - 0501 family are in use. The receiver type HFBR 2521 (blue) is used for the input signals TOP IN (U1) and BOT IN (U3). The transmitter type HFBR 1521 (grey) is used for the output ERROR OUT (U2). Please refer to the data sheet section for exact position of the F-option.

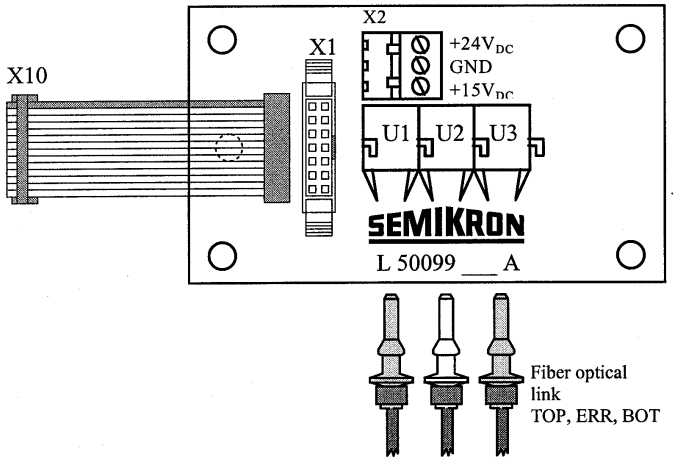


Fig. 19 F-Option

Accessories

Snubber Capacitors

SEMIKRON provides film capacitors which can be adapted onto the DC-terminals of the SKiiP systems. These capacitors reduce the over voltage peak during commutation. The suitability of the capacitor has to be checked for each application.

The table below lists the available types.

Capacitance/DC-voltage	recommended for use with	ID number
470 nF / 1000 V	1200 V Devices	41046230
220 nF / 1250 V	1700 V Devices	41046220

AC Busbars

The AC outputs of SKiiP GB circuits must be paralleled externally

SEMIKRON recommends dedicated bus bars for paralleling as shown below:

Item	ID number
AC-bar for GB-Type 2-fold	41034390
AC-bar for GB-Type 3-fold	41034400
AC-bar for GB-Type 4-fold	41034410

DC-Link Capacitors and Bus Bars

SEMIKRON supplies tested capacitors banks (see Fig. 20 for 1200 V-IGBT and Fig. 21 for 1700 V-IGBT) with low stray inductance for direct mounting onto the SKiiP. You can make a choice from the most common references:

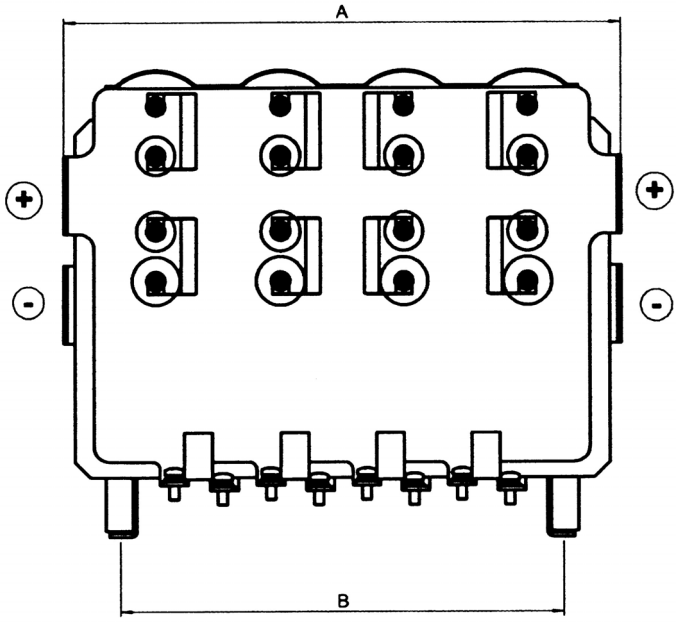
(Table DC-Link Capacitors and bus bars, see at the end of this chapter)

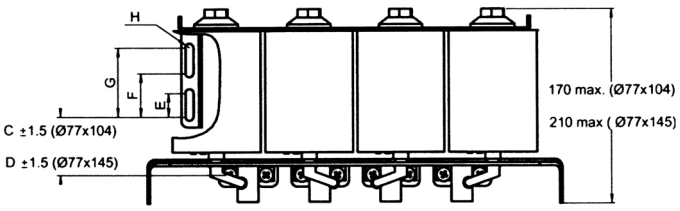
SEMIKRON electrolytic capacitors have been specified for a drive application usage. Please check the current in the capacitors for your own application before making a choice.

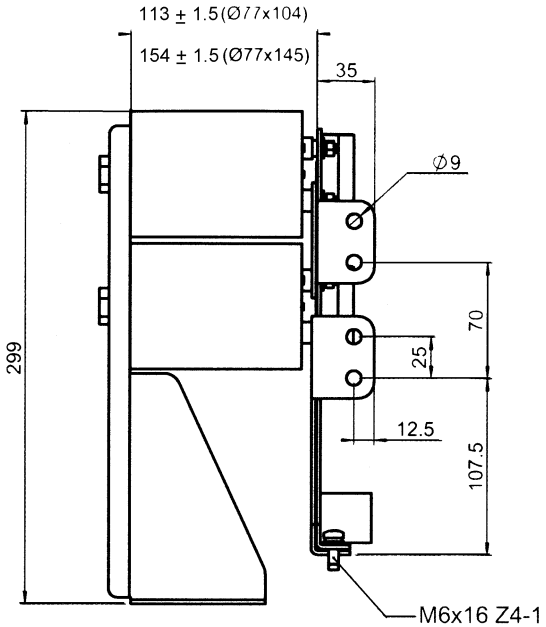
The following table gives the maximum ripple current per capacitor bank at 100 Hz, 85 °C, for 15 000 hours life time.

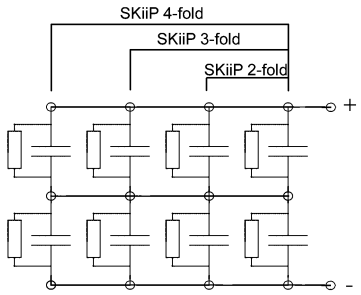
Voltage	Rated capacitance (µF)	Ripple current (A) (max. 100 Hz, 85 °C)
350	3300	10,9
400	2200	8,2
400	3300	10,1
400	4700	13,4
450	2200	8,8
450	3300	12,6
450	4700	14

The capacitor bank comes along with a reinforced support plate and the snubber capacitors. During assembly, great care should be taken to avoid any damage onto the sharing resistors.





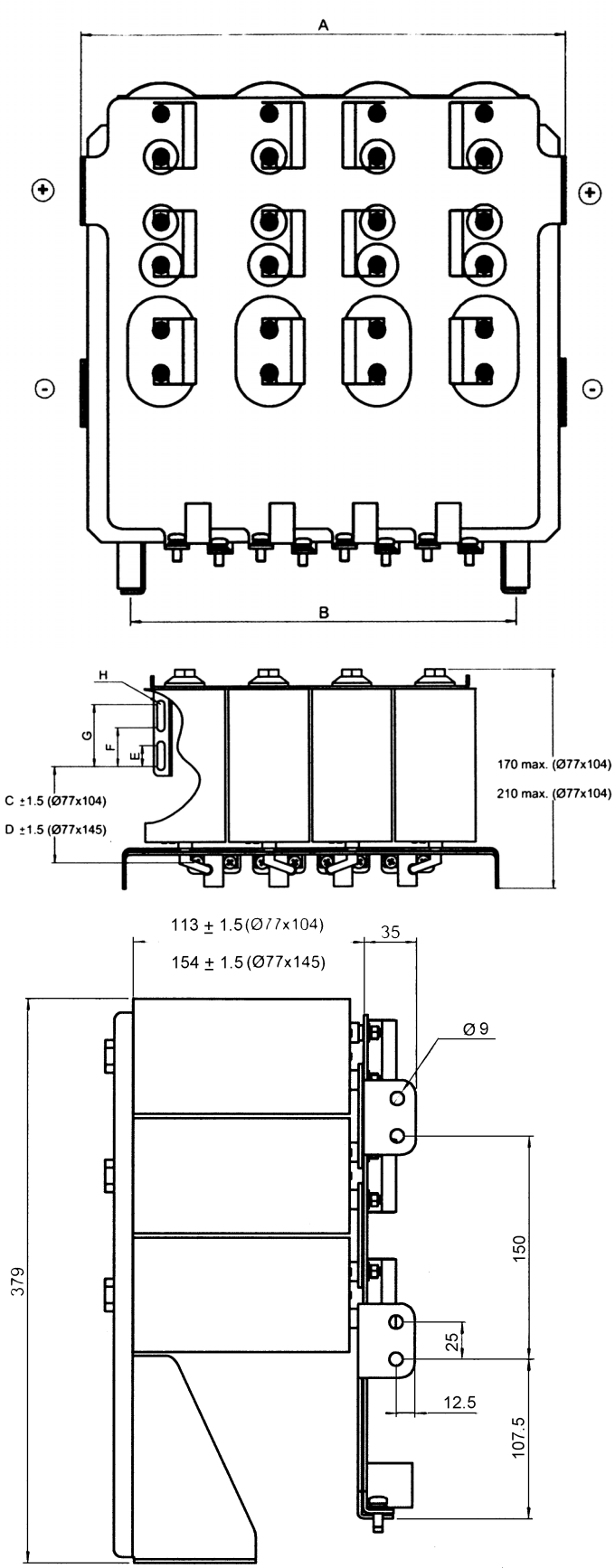


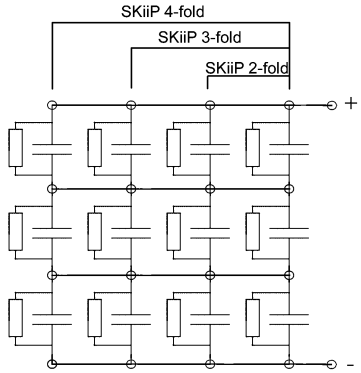


	A	B	C	D
SKiiP 2-fold	200	158	74,3	115,3
SKiiP 3-fold	280	226	50,3	91,3
SKiiP 4-fold	380	286	50,3	91,3

	E	F	G	H
SKiiP 2-fold	18	29	43	R 2,75
SKiiP 3-fold	20	37	59	R 3,5
SKiiP 4-fold	20	37	59	R 3,5

Fig. 20 DC Link Capacitor Bank for 1200V IGBTs





	A	B	C	D
SKiiP 2-fold	200	158	74,3	115,3
SKiiP 3-fold	280	226	50,3	91,3
SKiiP 4-fold	360	286	50,3	91,3

	E	F	G	H
SKiiP 2-fold	18	29	43	R 2,75
SKiiP 3-fold	20	37	59	R 3,5
SKiiP 4-fold	20	37	59	R 3,5

Fig. 21 DC Link Capacitor Bank for 1700V IGBTs

For further details on capacitor banks see also the separate capacitor datasheets.

Application Notes

Content

1 ESD Protection

Every SKiiP System is equipped with an ESD protective cover. To avoid any electrostatic discharge do not remove the protective cover before the SKiiP System is completely installed. Use conductive floor and grounded armbands during assembly.

2 Connections to power terminals

It is mandatory to use a low-inductive “sandwich” bus bar structure to connect the DC link to the DC-terminals of the SKiiP System. The DC link bank has to be designed this way that each DCB faces the same impedance to the voltage source respectively DC link bank. This way the current distribution is as even distributed. The usage of high frequency film capacitors (see also section accessories) on the DC link connections is necessary, to reduce the over voltages in case of a short circuit.
When a “GB” -type SKiiP System is used the AC terminals must be connected to each other. SEMIKRON provides suitable bus bars (see section accessories”). And again the AC terminals have to be connected as symmetric as possible to ensure the even current distribution.
To prevent EMI related disturbances the control signal connections shall be kept as far away as possible from the main connections (because of high dv/dt on the AC rails and high di/dt on the DC rails).
The torque level for DC and AC terminal screws as well as thread geometry is given in the datasheets.
The applied pulling forces in any direction on the terminals must be kept to a minimum. For that reason it is compulsory to take measures to reduce these forces. For the maximum allowed pull force per terminal on SKiiP modules refer to following table and figure 1.

Force	Maximum allowed force
F_{X+} / F_{-X}	< 100 N
F_{Y+} / F_{-Y}	< 100 N
F_{+Z}	< 100 N
F_{-Z}	< 200 N

Maximum allowed pulling force per terminal

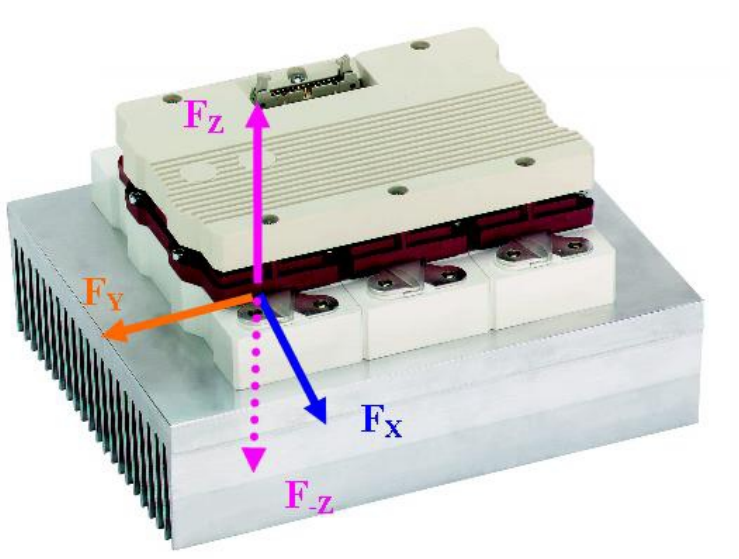


Fig. 1 Maximum allowed pull forces

In particular, forces added by thermal expansion, mechanical tolerances and peak power during system vibration must not exceed this limit. SEMIKRON strongly recommends to absorb mechanical forces by an external fixation point. In figure 2 a design proposal is given:

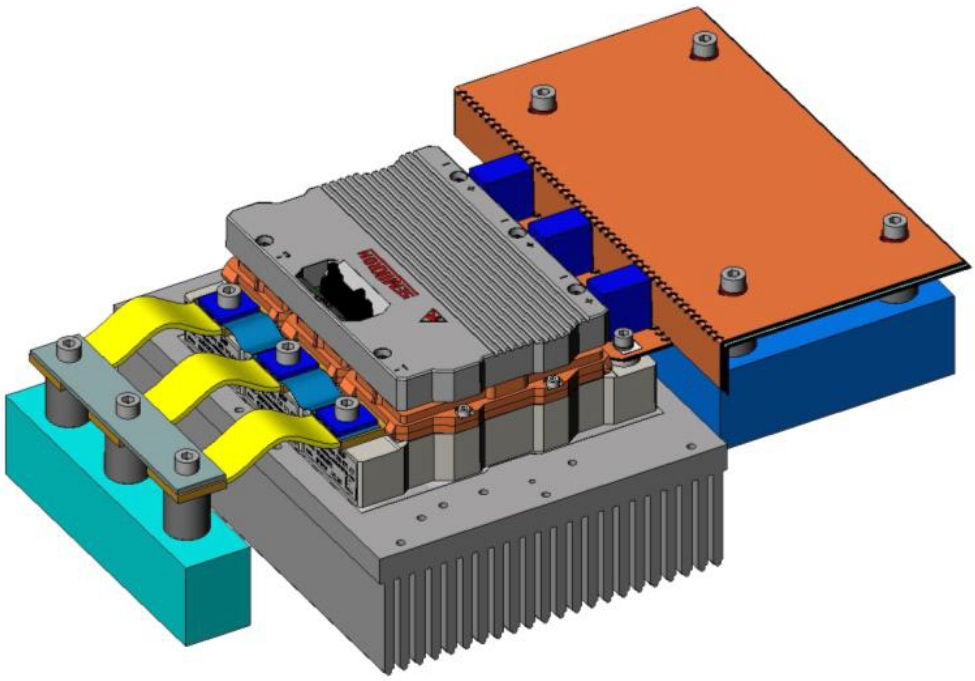


Fig. 2 Recommendation of AC/DC bus bar design for SKiiP (capacitors are not shown)

SEMIKRON recommends to use fixing posts to relieve the force on the SKiiP AC and DC terminals. The poles shall be mounted directly on to the heat sink or a fixed frame construction and placed close to the SKiiP device. Forces caused by the DC link capacitor bank or the weight of the load cables have to be absorbed by the mechanical construction.

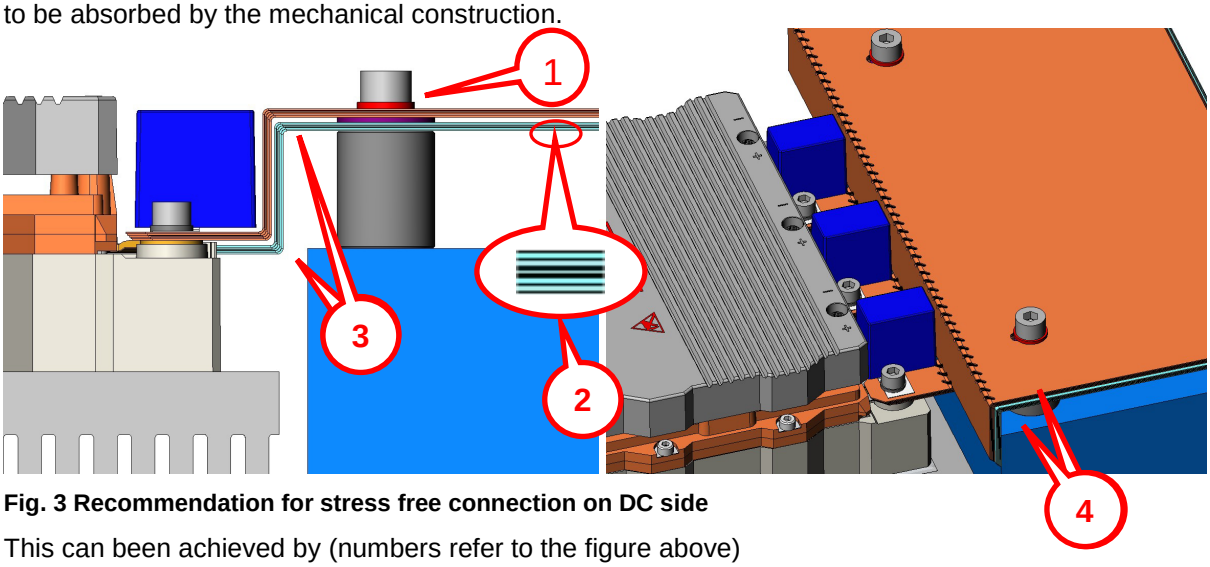


Fig. 3 Recommendation for stress free connection on DC side

This can been achieved by (numbers refer to the figure above)

1. isolating **fixing post** (mounted on frame or the like) → decoupling of external forces
2. thin **laminar metal sheets** → more flexibility
3. **bending** in DC laminar rail → this way horizontal movements of the capacitor bank can not be distributed to the terminals
4. **slits** in DC metal sheets → more flexibility (Please note that the slits can increase the terminal temperature due to higher conduction losses). Especially for several SKiiP at the same DC-Link and on the same heat sink, there has to be a flexible connection which can take over the mechanical stress caused by mechanical tolerances and thermal extensions.

To ensure a mechanical stress free AC terminal connection it is recommended to use flexible cables or flexible layers which are fixed on poles in front of the connectors (see also www.mettex.com or www.sefag.ch). Figure 4 shows how this can be achieved on the AC side.

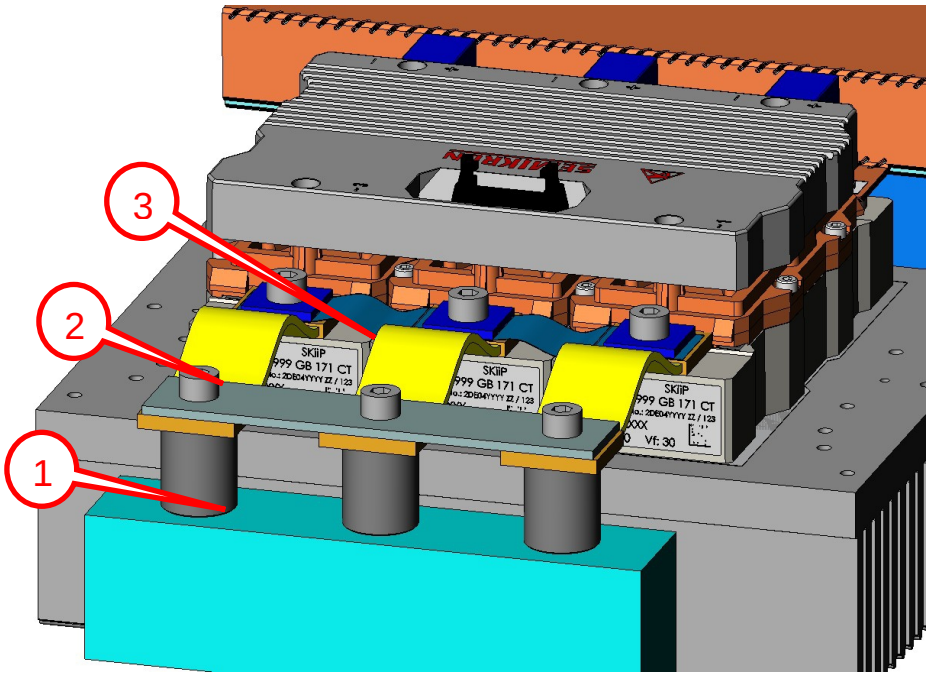


Fig. 4 Recommendation for mechanical stress free AC connections

The robustness has been obtained by (numbers refer to the figure above):

1. isolating **fixing post** (mounted on heat sink or the like) → decouples external forces
2. AC connections with flexible high current **copper braid** → gives more flexibility
3. Low inductive parallel connection of the AC terminals for SKiiP GB types of 2 to 4 power sections. This connection is represented in the diagram (Fig. 5) by Lp13 and Lp23. These inductances represent the influence of the copper-braid (yellow) and the cross connectors (grey). This inductance needs to be realized symmetric and low to avoid coupling effects across the auxiliary emitter (Resym1 and Resym2) of the TOP IGBT. The above mentioned coupling effects in the emitter path of the paralleled DCBs may cause switching oscillations of the TOP IGBT during switching events between the DCBs. It becomes severe for AC connections which are longer then approx. 5cm from the AC terminal away. To reduce this inductance can be achieved low by an additional flexible **cross connector** directly mounted on the SKiiP AC terminals (see reference number 3 in Figure 4). Please note that the current rating of this bar must not be very high, because there is no load current flowing in this bar. There are only high frequency currents flowing. Thus the flexibility can be achieved by using a comparatively thin material.

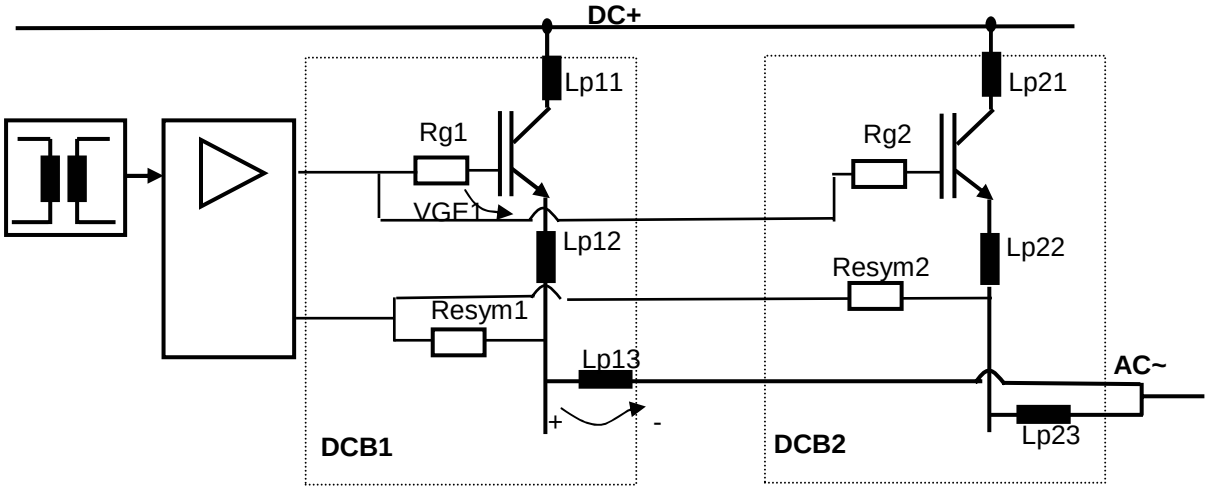


Fig. 5 Topology of a 2 bay SKiiP (driver and power components for TOP IGBT)

The rating and cooling of the load cables and the dc link bank must be carried out in that way that no thermal energy is fed into the SKiiP. For that reason the terminal temperature on the AC terminals

shall not exceed 115°C at 400A_{rms} and 70°C heat sink temperature. For the dc link terminals the temperature shall not exceed 115°C at 280A_{rms} and 70°C heat sink temperature.
The AC outlet of SKiiP3 has a different position compared to SKiiP2; please refer to the data sheet for exact position.

3 Connection to the Signal Terminals of the Gate Driver

The standard connection to a SKiiP System is done via a DIN 41651 connector. Because of voltage drop and for immunity against electromagnetic interference the maximum length of the flat cable should not exceed 3 meters. To avoid interferences, the flat cable should be placed as far as possible away from the power terminals, the power cables, the DC-link capacitors and all other noise sources. We recommend to keep the ribbon cables as close to GND as possible (e.g. heat sink or the like).
Because of the EMC conception of the driver board the usage of expensive screened flat ribbon cables is in many applications not needed. However in noise intensive applications it is recommended to improve the noise immunity with screened cable or the usage of fibre optical interfaces.

4 Environmental Restrictions

Humidity and climate class are shown in the data sheets. The documented classes specify the restrictions for operation, storage and transport of SKiiP Systems.

5 Parallel Operation of „GB“-type SKiiP Systems

In applications where paralleling of 2,3 or more GB type SKiiP systems is necessary, it has to be made sure that no in-homogenous current distribution occurs. The reasons for this can be:

- different propagation time of driver boards (jitter of approx. 0...150ns)
- different switching times of power semiconductors
- tolerance of forward voltage drop of IGBT or diodes
- unsymmetrical current distribution in the AC bus bars
- different cooling conditions of paralleled half bridges (e.g. in air cooled applications with thermal stacking)

The system designer has to make sure that there is sufficient inductance (a few µH should be in most applications sufficient) between the AC output terminals of the paralleled „GB“-type SKiiP Systems to avoid inhomogeneous current distribution.
The inductance L might be realized by iron powder ferrites (e.g. COROVAC). The required inductance depends on DC voltage, allowable “cross” current and the propagation time differences of the paralleled “GB”-type SKiiP Systems. To prevent mechanical stress because of tolerances and thermal extension there should not be used a stiff connection between the AC terminals of the individual SKiiPs.
For a maximum deviation of the maximum rated output current the inductance has to be rated with a minimum value as shown in Figure 6.
For Example in an application with V_{CC}= 900V, I_{outmax}= 2x600A = 1200A, a permissible current deviation of 10% of the overall current the minimum value of the inductor is:

$$L_{\min} = \frac{900V * 150ns}{10\% * 1200A} = 1{,}1\mu H$$

It has to be taken into account that for in-homogenous current sharing a de-rating of the nominal current of the power modules have to be considered (e.g. in the case above 1200A output current are needed, thus the modules have to be rated for the (600A each + 10%* 1200A) = 720A).

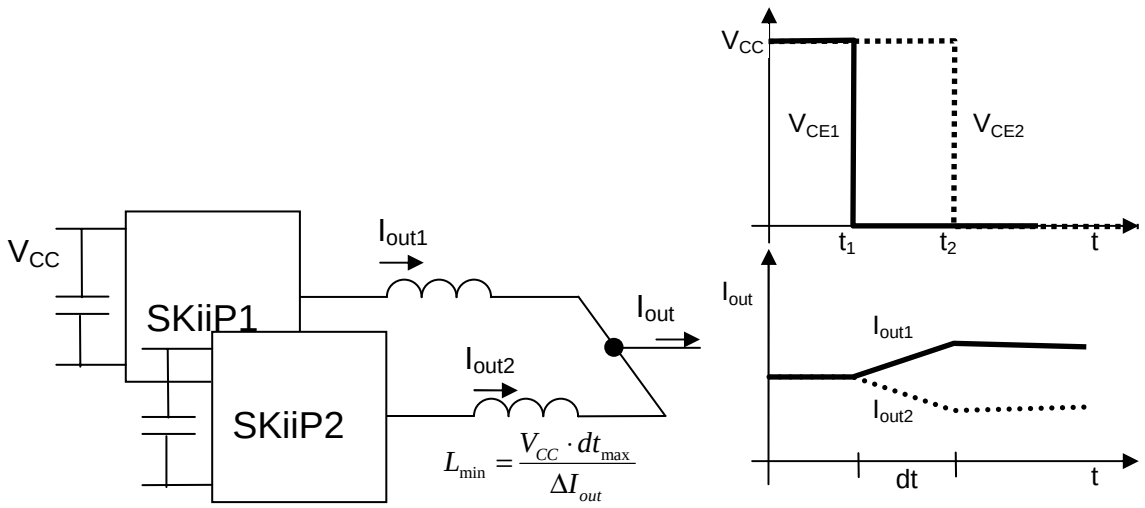


Fig. 6 Paralleled SKiiPs

6 Minimum turn–on time for free wheeling diodes

When a semiconductor is turned-on, charge carriers need a specific time to spread across the chip area to set the semiconductor into the "on-state". When during this transient state a switching event happened, it may result in a

- higher di/dt compared to fully turned-on devices
- to overvoltages
- the diode can show a „snap off" behaviour with oscillations

To prevent this, a minimum turn-on time for the diodes (corresponds with inductive load to the turn-off times for IGBT → "BOT IN" or "TOP IN" = Low) of

- 3µs for 1200V devices and
- 5µs for 1700V devices

is recommended.

Please note: If inverted signals are used for "BOT IN" and "TOP IN", than the SKiiP interlock time sets the minimum "off-time" for the IGBT already to 3,3µs.

7 Fusing of Large DC-Link-Capacitor Banks

For high power applications with several SKiiP at one DC-Link it is recommended to separate each individual SKiiP and it's DC-Link-Capacitor with fuses from the other energy sources/DC-Link-Capacitors.

8 Electro-Magnetic Interference

The EMI relevant behavior is determined by the switching behavior on the one hand and on the coupling characteristic to the surrounding environment on the other hand (see also application handbook).

With SKiiP3 a new generation of silicon is introduced, which reduces the total loss per ampere output current compared to SKiiP2 and therefore shows different switching characteristics versus SKiiP2. This must be taken into account when SKiiP2 is replaced by SKiiP3.

The ceramic substrate area of SKiiP3 is increased towards SKiiP2. Therefore the capacitive coupling between heat sink and SKiiP3 is higher (please refer to data sheet parameter C_{CHC}).

The coupling capacitance of SKiiP between the driver primary and secondary side is determined by the signal and the DCDC transformers. The values can be seen in the following table.

	GD	**GB**
$\mathbf{C_{prim\text{-}sec}}$	3x10pF	2x10pF

9 Usage of Water Cooled Heat Sinks

For the usage of water cooled heat sinks we recommend to take care of the following points:

- Always ensure to use the correct concentration of cooling liquid (for details see data sheets). In case that the concentration of corrosion-inhibitors is too low, corrosion as consequential damage may occur.
- For high temperature differences between ambient air temperature and water cooler please consider that there no condensate liquid damages the system.
- Please ensure that the cooling liquid is suitable for all metal parts in the cooling circuit (e.g. steel, aluminum, other non-ferrous metals)
- It should be used water, which has been de-ionized (e.g. chlorine ions can accelerate the corrosion)
- The water hardness shall be kept to a minimum, to avoid scale. Please note that scale increase the thermal resistance.
- The O_2 content has to be kept to a minimum by a closed cooling circuit to avoid corrosion.

10 Further Application Support

For electrical and thermal design support please use SEMISEL. under SEMIKRON website http://semisel.semikron.com or read the SEMIKRON application hand book (also available under http://www.semikron.com).

PIN-array - halfbridge driver SKiiP 2, 3 GB 2, 3, 4-fold

X1:

Pin	signal	remark
1	shield	
2	BOT IN[2)]	positive 15V CMOS logic; 10 kΩ impedance, don´t connect when using fiber optic
3	ERROR OUT[1)]	LOW = NO ERROR; open Collector Output; max. 30 V / 15 mA don´t connect when using fiber optic, propagation delay 1 µs min. pulsewidth error-memory-reset 9 µs
4	TOP IN[2)]	positive 15V CMOS logic; 10 kΩ impedance don´t connect when using fiber optic
5	Overtemp. OUT[1)]	LOW = NO ERROR = ϑ_{DCB} < 115 ± 5°C open collector Output; max. 30 V / 15 mA „low“ output voltage < 0,6 V „high“ output voltage max. 30 V
6	+ 24 V_{DC} IN	24 V_{DC} (SKiiP 2: 20 - 30 V, SKiiP 3: 13 - 30 V)
7	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DCIN} supply voltage monitoring threshold 19,5 V
8	+ 15 V_{DC} IN (SKiiP 2 only)	15 V_{DC} ± 4 % power supply
9	+ 15 V_{DC} IN (SKiiP 2 only)	don´t supply with 15 V, when using + 24 V_{DCIN} supply voltage monitoring threshold 13 V
8	+ 15 V_{DC} OUT	max. 50 mA auxiliary power supply when
9	+ 15 V_{DC} OUT	SKiiP system is supplied via pin 6/7
10	GND	GND for power supply and
11	GND	GND for digital signals
12	Temp. analog OUT or U_{DC} analog OUT[3)]	U_{DC} when using option “U” actual DC-link voltage, 9 V refer to U_{DCmax} max. output current 5 mA; overvoltage trip level 9 V
13	GND aux	reference for analog output signals
14	I analog OUT	**SKiiP 2 and SKiiP 3 with Al_2O_3 ceramic substrate** current actual value 8,0 V ⇔ 100 % I_C @ 25 °C overcurrent trip level 10 V ⇔ 125 % I_C @ 25 °C current value > 0 ⇔ SKiiP system is source current value < 0 ⇔ SKiiP system is sink **SKiiP 3 with AlN ceramic substrate:** refer to corresponding datasheet

1) Open collector output, external pull up resistor necessary
2) „high“ (max) 12,3 V, „low“ (min) 4,6 V; SKiiP 3: 1 nF capacitance added signal to GND
3) When using option “U” the analog temperature signal is not available

PIN-array - 3-phase bridge driver SKiiP 2, 3 type „GD”

X1:

Pin	signal	remark
1	shield	
2	BOT HB 1 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
3	ERROR HB 1 OUT [1)]	short circuit monitoring HB1 LOW = NO ERROR; open collector output; max. 30 V / 15 mA propagation delay 1 µs, min. pulsewidth error-memory-reset 9 µs
4	TOP HB 1 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
5	BOT HB 2 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
6	ERROR HB 2 OUT [1)]	short circuit monitoring HB2 LOW = NO ERROR; open collector output; max. 30 V / 15 mA propagation delay 1 µs, min. pulsewidth error-memory-reset 9 µs
7	TOP HB 2 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
8	BOT HB 3 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
9	ERROR HB 3 OUT [1)]	short circuit monitoring HB 3 LOW = NO ERROR; open collector output; max. 30 V / 15 mA propagation delay 1 µs, min. pulsewidth error-memory-reset 8 µs
10	TOP HB 3[2)]	positive 15V CMOS logic; 10 kΩ impedance
11	Overtemp. OUT [1)]	LOW = NO ERROR = ϑ_{DCB} < 115 ± 5°C open collector Output; max. 30 V / 15 mA „low“ output voltage < 0,6 V „high“ output voltage max. 30 V
12	reserved	
13	U_{DC} analog OUT	U_{DC} when using **option „U”** actual DC-link voltage, 9,0 V refer to U_{DCmax} max. output current 5 mA
14	+ 24 V_{DC} IN	24 V_{DC} (SKiiP 2: 20 - 30 V, SKiiP 3: 13 - 30V)
15	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DC} (SKiiP 2 only)
16	+ 15 V_{DC} IN (SKiiP 2 only)	15 V_{DC} ± 4 % power supply
17	+ 15 V_{DC} IN (SKiiP 2 only)	don´t supply with 15V, when using +24V_{DCIN} supply voltage monitoring threshold 13 V
16	+ 15 V_{DC} OUT	max. 50 mA auxiliary power supply when
17	+ 15 V_{DC} OUT	SKiiP system is supplied via pin 14/15
18	GND	GND for power supply and
19	GND	GND for digital signals
20	Temp. analog OUT	max. output current 5 mA
21	GND aux	
22	I analog OUT HB 1	**SKiiP 2 and SKiiP 3 with Al_2O_3 ceramic substrate:** current actual value 8,0 V ⇔ 100 % I_C @ 25 °C overcurrent trip level 10 V ⇔ 125 % I_C @ 25 °C current value > 0 ⇔ SKiiP is source current value < 0 ⇔ SKiiP is sink **SKiiP 3 with AlN ceramic substrate:** refer to corresponding datasheet
23	GND aux	reference for analog output signals
24	I analog OUT HB 2	as pin 22
25	GND aux	reference for analog output signals
26	I analog OUT HB 3	as pin 22

1) Open collector output, external pull up resistor necessary
2) „high“ (max) 12,3 V, „low“ (min) 4,6 V; SKiiP 3: 1 nF capacitance added signal to GND

PIN-array - brake chopper driver (used in SKiiP 2 type GDL)

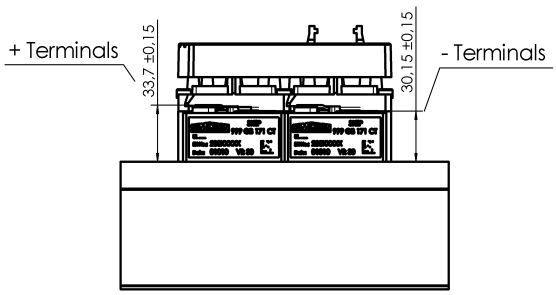
X2:

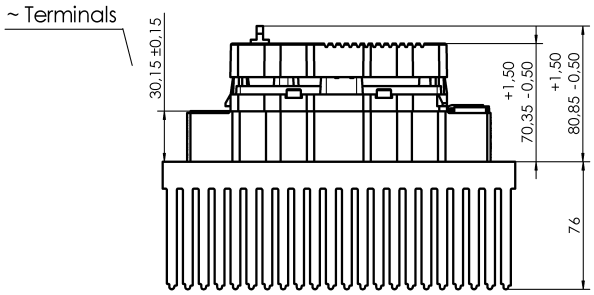
Pin	signal	remark
1	shield	connected to GND (for usage of shielded cable)
2	CHOPPER ext. ON	LOW = IGBT ON „low“ (max) 5 V, I_{min} = 5 mA „high“ (min) 11,5 V propagation delay $t_{d(on)} \leq 20\ \mu s$ $t_{d(off)} \leq 25\ \mu s$
3	ERROR OUT[1)]	LOW = NO ERROR open collector Output; max. 30 V / 2,5 mA propagation delay$t_{PD(on)error} \leq 60\ \mu s$
4	RESET	LOW = RESET Reset-pulse-time $t_{PDRESET}$ > 300 ms connect this pin to open collector output **without** pull up resistor „low“ (max) 2 V, „high“ (min) 12 V
5	reserved	
6	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DCIN} supply voltage monitoring threshold 15,6 V
7	+ 24 V_{DC} IN	
8	+ 15 V_{DC} IN	don´t supply with 15 V, when using + 24 V_{DCIN} supply voltage monitoring threshold 13 V
9	+ 15 V_{DC} IN	
10	GND	
11	GND	
12	reserved	
13	reserved	
14	reserved	

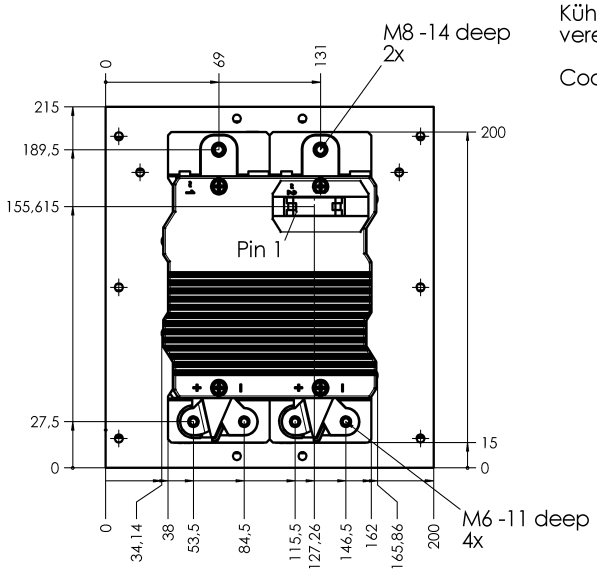
[1)] Open collector output, external pull up resistor necessary

SKiiP 3

Case S 23 mounted on PX16 heat sink

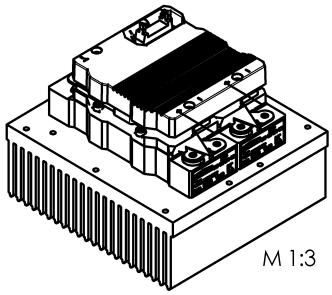






Kühlkörperdarstellung
vereinfacht

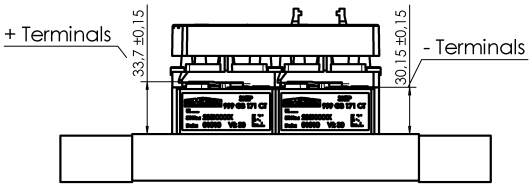
Cooler simpified

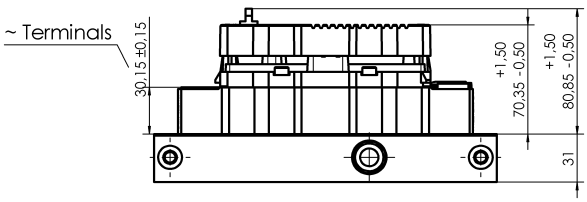


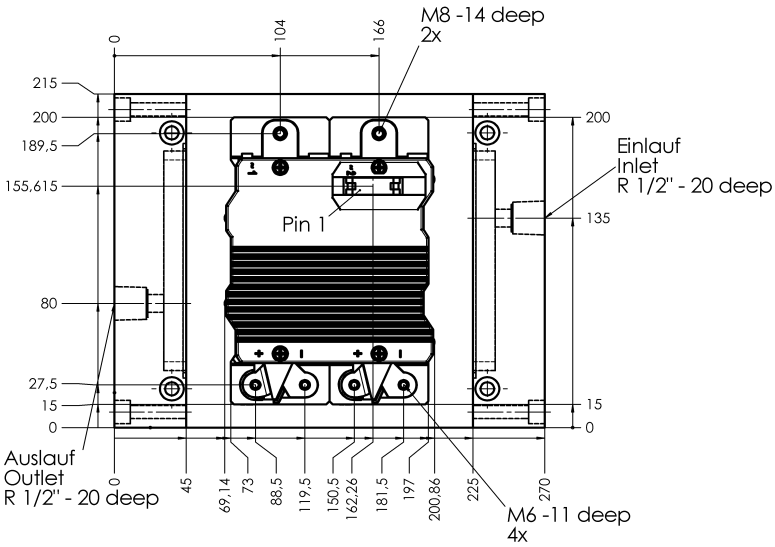
weight without heat sink: 1,7 kg

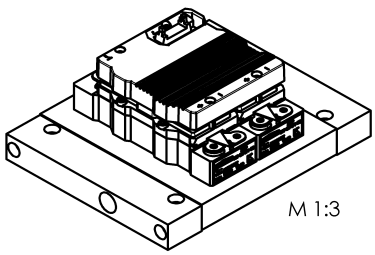
PX 16/200: 5,4 kg

Case S 23 mounted on liquid cooled heat sink NWK 40





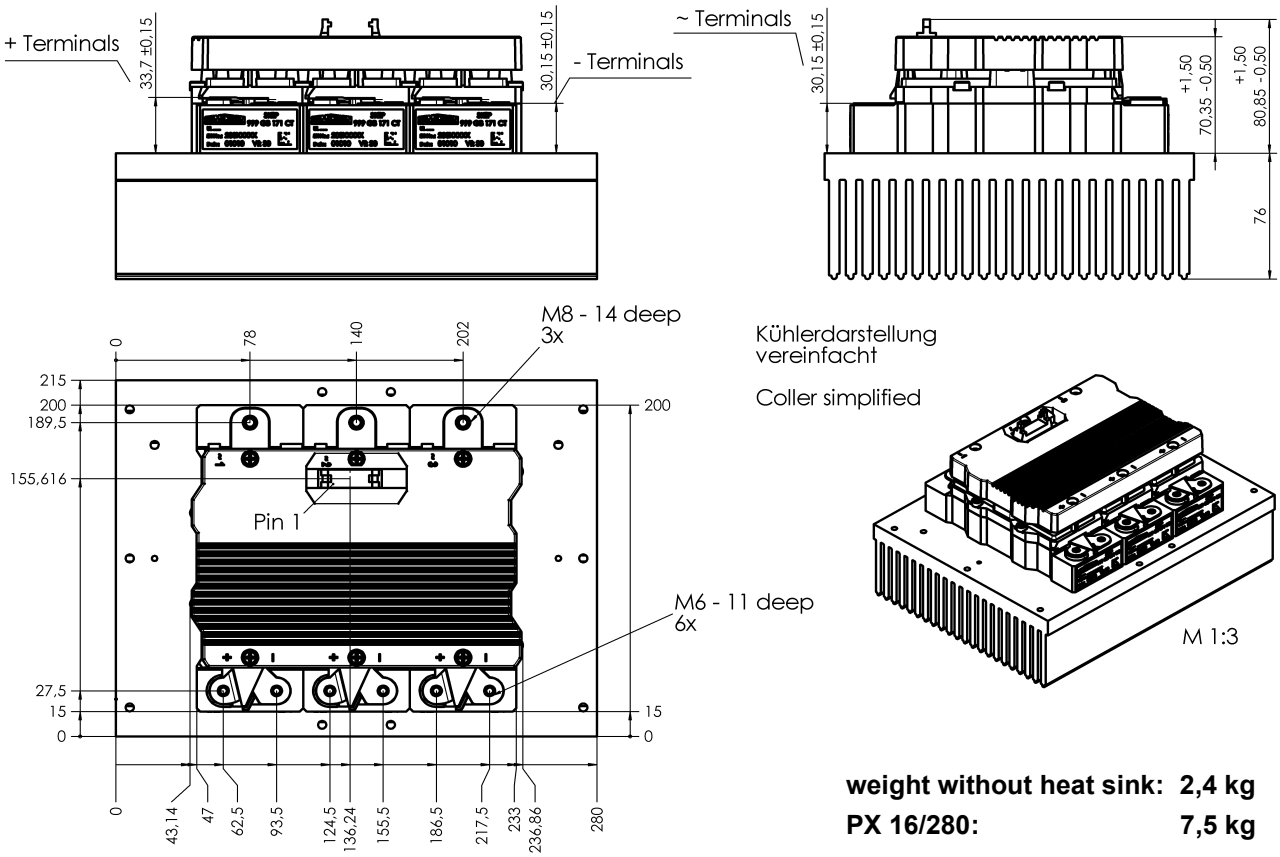




NWK 40/180: 6,5 kg

SKiiP 3

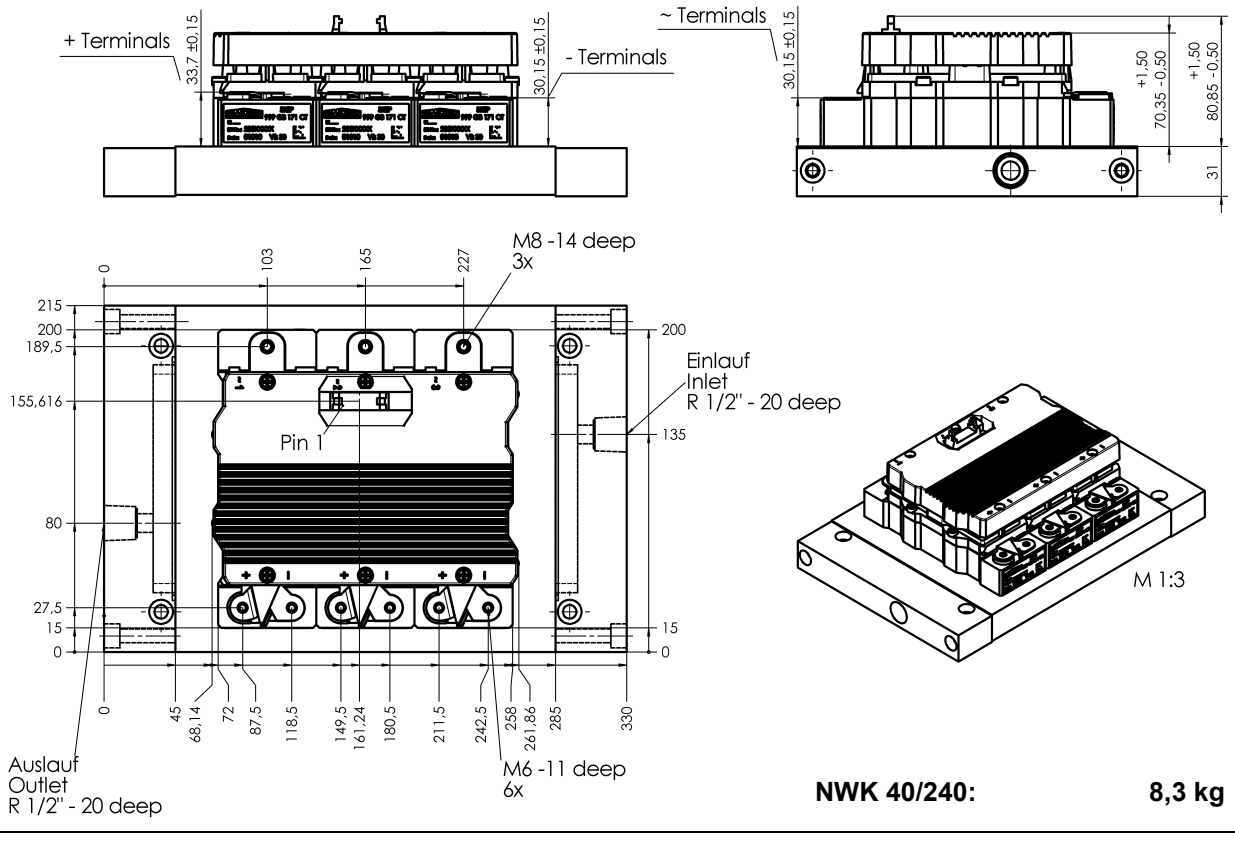
Case S 33 mounted on PX16 heat sink



weight without heat sink: 2,4 kg

PX 16/280: 7,5 kg

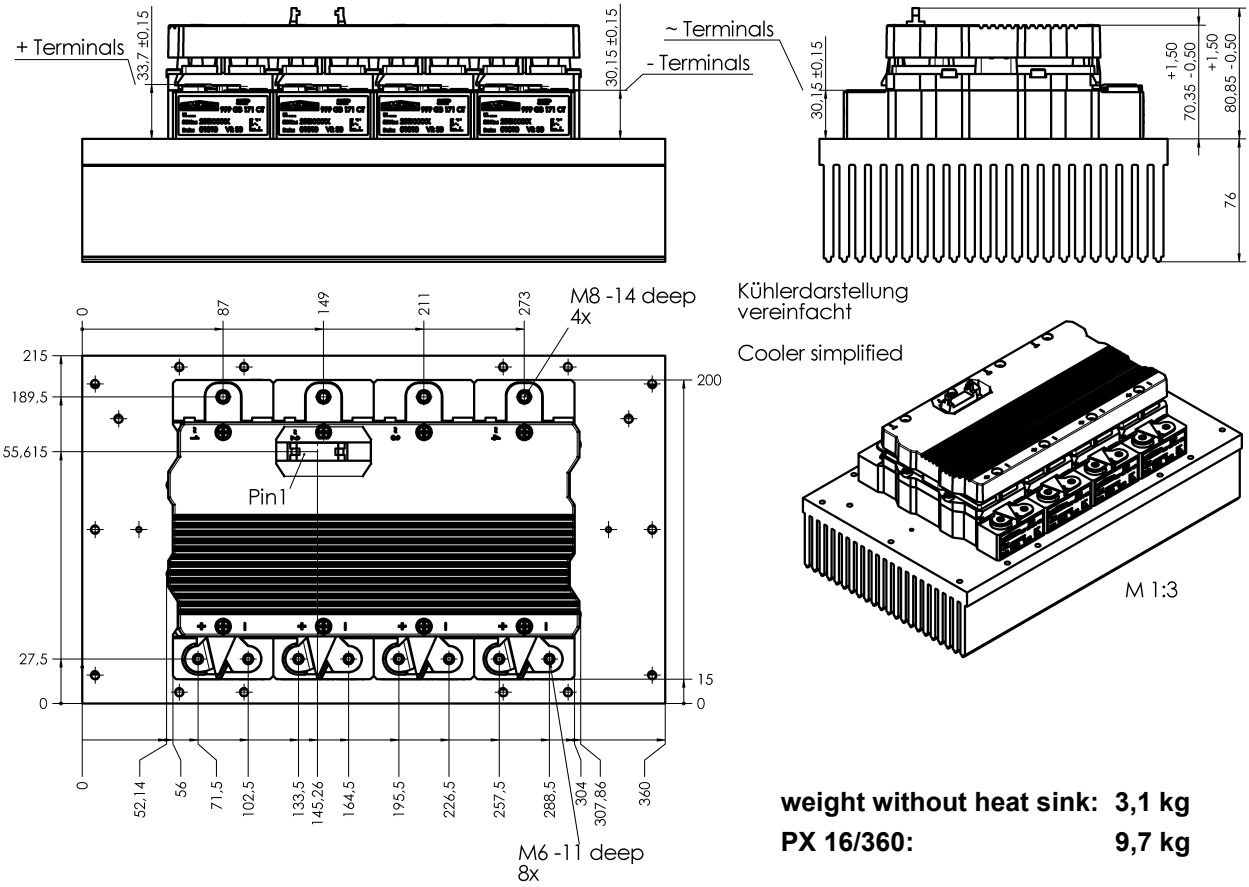
Case S 33 mounted on liquid cooled heat sink NWK 40



NWK 40/240: 8,3 kg

SKiiP 3

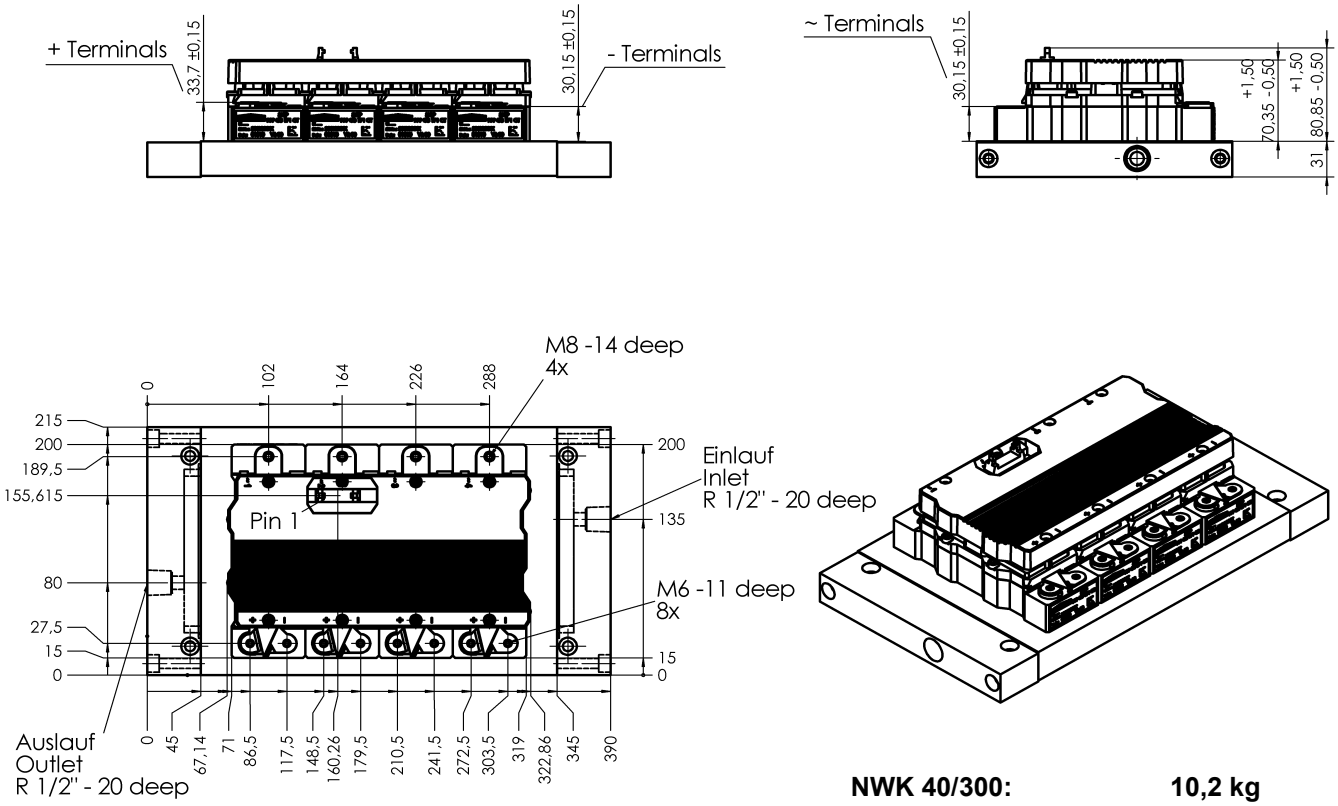
Case S 43 mounted on PX16 heat sink



weight without heat sink: 3,1 kg

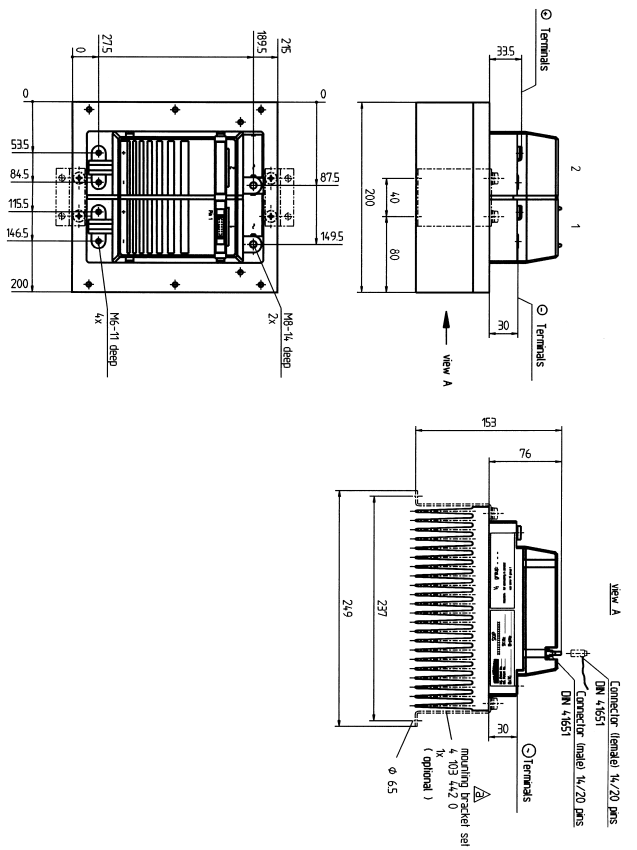
PX 16/360: 9,7 kg

Case S 43 mounted on liquid cooled heat sink NWK 40



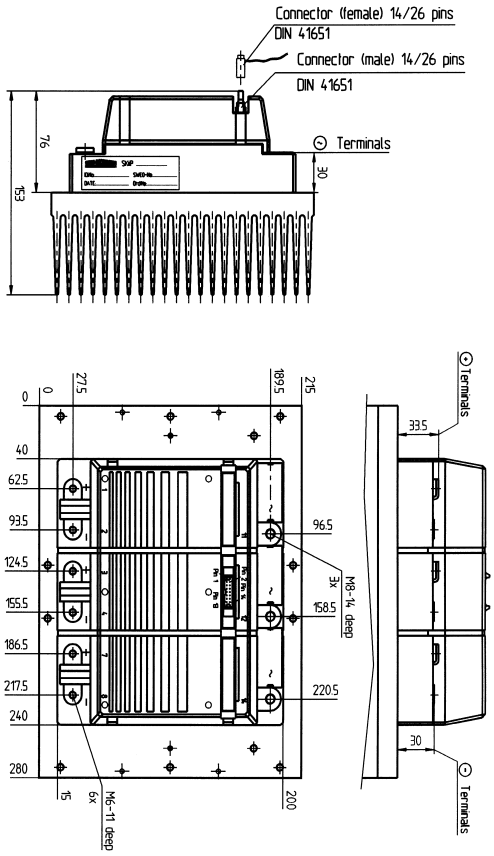
NWK 40/300: 10,2 kg

Case S2 **SKiiP 2 GB 2-fold**



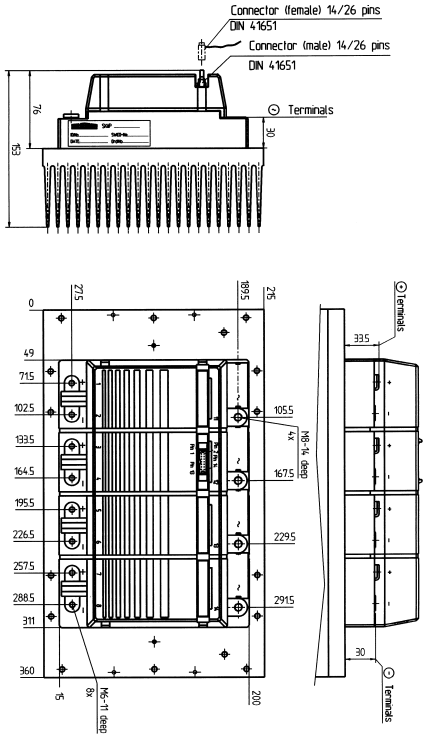
weight without heat sink: 1,85 kg
P16: 4,7 kg

Case S3 **SKiiP 2 GB 3-fold**



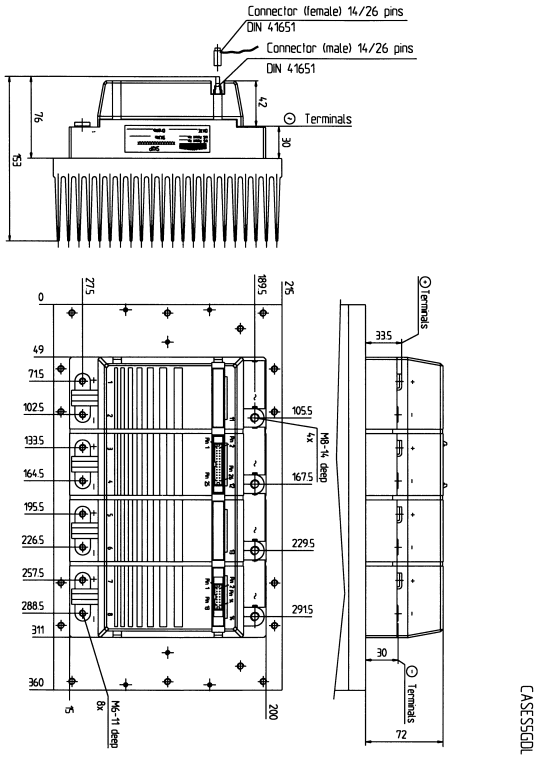
weight without heat sink: 2,72 kg
P16: 6,6 kg

Case S4 **SKiiP 2 GB 4-fold**



weight without heat sink: 3,54 kg
P16: 8,46 kg

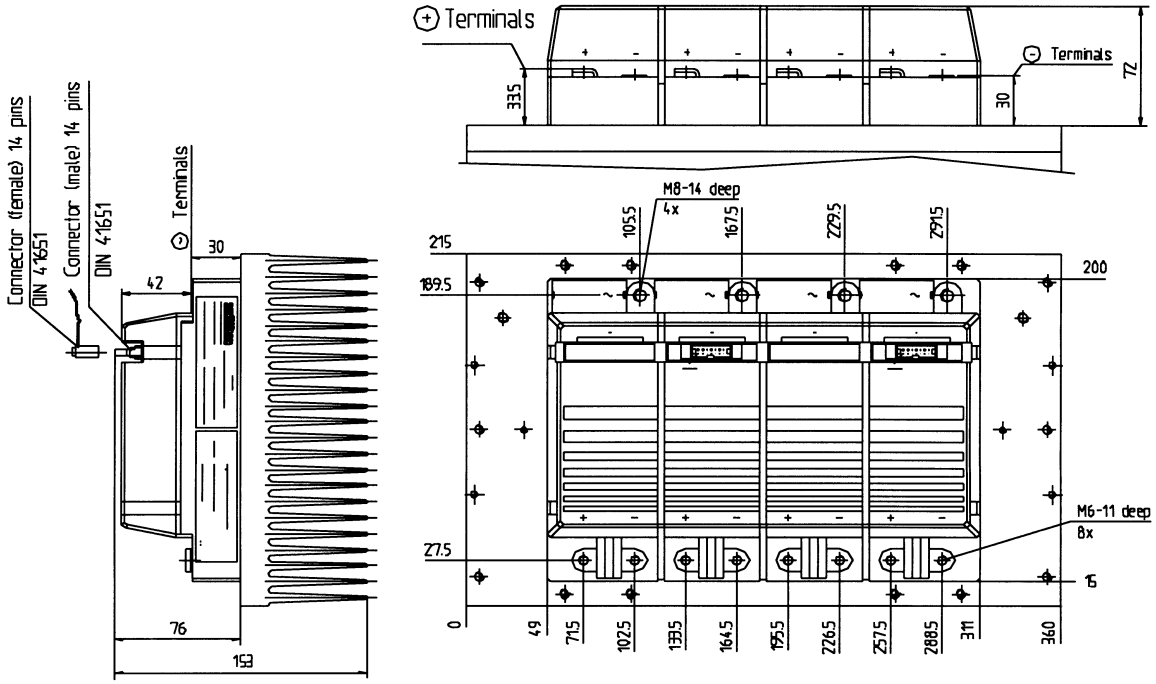
Case S5 **SKiiP 2 GDL 4-fold**



weight without heatsink: 3,54 kg
P16: 8,46 kg

Case S5 **SKiiP 2 2*GB 2-fold**

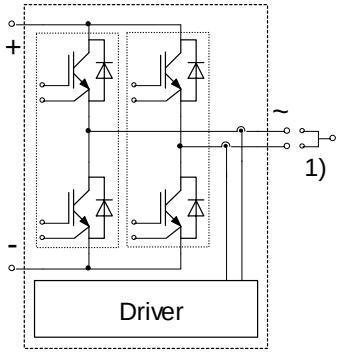
CASES5GH



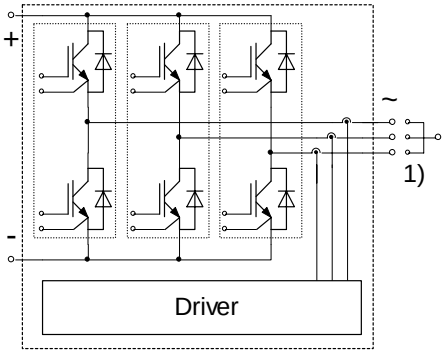
weight without heat sink: 3,54 kg
P16: 8,46 kg

Circuit Diagrams

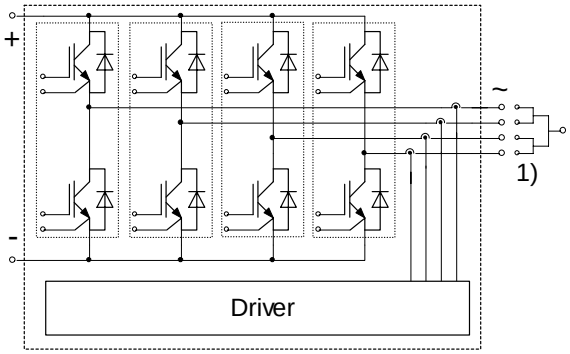
SKiiP: 2-fold „GB“ (Case S2; S23)



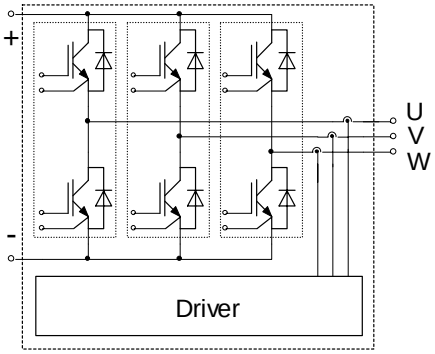
SKiiP: 3-fold „GB“ (Case S3; S33)



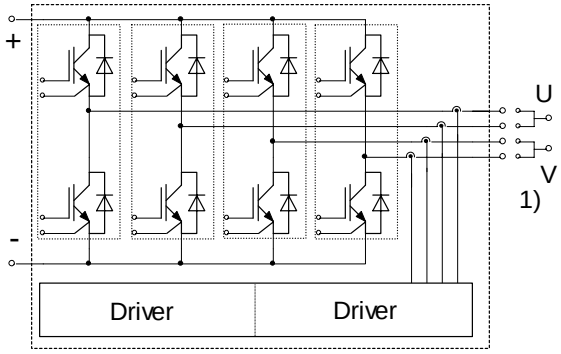
SKiiP: 4-fold „GB“ (Case S4; S43)



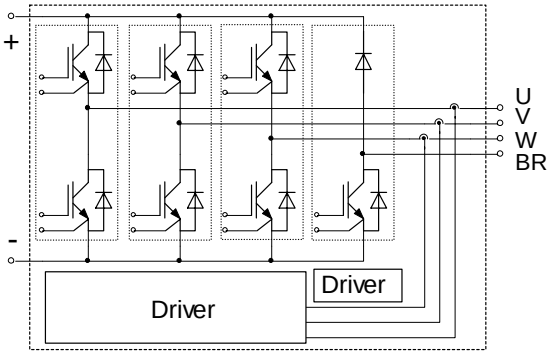
SKiiP: 3-fold „GD“ (Case S3; S33)



only SKiiP2: 4-fold „GH“ (Case S5GH)



only SKiiP2: 4-fold „GDL“ (Case S5GDL)



1) AC connection busbars must be connected by the user, busbars for 2-,3- and 4-fold SKiiP are available on request