PIN-array - halfbridge driver SKiiP 2, 3 GB 2, 3, 4-fold

X1:

Pin	signal	remark
1	shield	
2	BOT IN[2)]	positive 15V CMOS logic; 10 kΩ impedance, don´t connect when using fiber optic
3	ERROR OUT[1)]	LOW = NO ERROR; open Collector Output; max. 30 V / 15 mA don´t connect when using fiber optic, propagation delay 1 µs min. pulsewidth error-memory-reset 9 µs
4	TOP IN[2)]	positive 15V CMOS logic; 10 kΩ impedance don´t connect when using fiber optic
5	Overtemp. OUT[1)]	LOW = NO ERROR = ϑ_{DCB} < 115 ± 5°C open collector Output; max. 30 V / 15 mA „low“ output voltage < 0,6 V „high“ output voltage max. 30 V
6	+ 24 V_{DC} IN	24 V_{DC} (SKiiP 2: 20 - 30 V, SKiiP 3: 13 - 30 V)
7	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DCIN} supply voltage monitoring threshold 19,5 V
8	+ 15 V_{DC} IN (SKiiP 2 only)	15 V_{DC} ± 4 % power supply
9	+ 15 V_{DC} IN (SKiiP 2 only)	don´t supply with 15 V, when using + 24 V_{DCIN} supply voltage monitoring threshold 13 V
8	+ 15 V_{DC} OUT	max. 50 mA auxiliary power supply when
9	+ 15 V_{DC} OUT	SKiiP system is supplied via pin 6/7
10	GND	GND for power supply and
11	GND	GND for digital signals
12	Temp. analog OUT or U_{DC} analog OUT[3)]	U_{DC} when using option “U” actual DC-link voltage, 9 V refer to U_{DCmax} max. output current 5 mA; overvoltage trip level 9 V
13	GND aux	reference for analog output signals
14	I analog OUT	**SKiiP 2 and SKiiP 3 with Al_2O_3 ceramic substrate** current actual value 8,0 V ⇔ 100 % I_C @ 25 °C overcurrent trip level 10 V ⇔ 125 % I_C @ 25 °C current value > 0 ⇔ SKiiP system is source current value < 0 ⇔ SKiiP system is sink **SKiiP 3 with AlN ceramic substrate:** refer to corresponding datasheet

1) Open collector output, external pull up resistor necessary
2) „high“ (max) 12,3 V, „low“ (min) 4,6 V; SKiiP 3: 1 nF capacitance added signal to GND
3) When using option “U” the analog temperature signal is not available

PIN-array - 3-phase bridge driver SKiiP 2, 3 type „GD”

X1:

Pin	signal	remark
1	shield	
2	BOT HB 1 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
3	ERROR HB 1 OUT [1)]	short circuit monitoring HB1 LOW = NO ERROR; open collector output; max. 30 V / 15 mA propagation delay 1 µs, min. pulsewidth error-memory-reset 9 µs
4	TOP HB 1 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
5	BOT HB 2 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
6	ERROR HB 2 OUT [1)]	short circuit monitoring HB2 LOW = NO ERROR; open collector output; max. 30 V / 15 mA propagation delay 1 µs, min. pulsewidth error-memory-reset 9 µs
7	TOP HB 2 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
8	BOT HB 3 IN[2)]	positive 15V CMOS logic; 10 kΩ impedance
9	ERROR HB 3 OUT [1)]	short circuit monitoring HB 3 LOW = NO ERROR; open collector output; max. 30 V / 15 mA propagation delay 1 µs, min. pulsewidth error-memory-reset 8 µs
10	TOP HB 3[2)]	positive 15V CMOS logic; 10 kΩ impedance
11	Overtemp. OUT [1)]	LOW = NO ERROR = ϑ_{DCB} < 115 ± 5°C open collector Output; max. 30 V / 15 mA „low“ output voltage < 0,6 V „high“ output voltage max. 30 V
12	reserved	
13	U_{DC} analog OUT	U_{DC} when using **option „U”** actual DC-link voltage, 9,0 V refer to U_{DCmax} max. output current 5 mA
14	+ 24 V_{DC} IN	24 V_{DC} (SKiiP 2: 20 - 30 V, SKiiP 3: 13 - 30V)
15	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DC} (SKiiP 2 only)
16	+ 15 V_{DC} IN (SKiiP 2 only)	15 V_{DC} ± 4 % power supply
17	+ 15 V_{DC} IN (SKiiP 2 only)	don´t supply with 15V, when using +24V_{DCIN} supply voltage monitoring threshold 13 V
16	+ 15 V_{DC} OUT	max. 50 mA auxiliary power supply when
17	+ 15 V_{DC} OUT	SKiiP system is supplied via pin 14/15
18	GND	GND for power supply and
19	GND	GND for digital signals
20	Temp. analog OUT	max. output current 5 mA
21	GND aux	
22	I analog OUT HB 1	**SKiiP 2 and SKiiP 3 with Al_2O_3 ceramic substrate:** current actual value 8,0 V ⇔ 100 % I_C @ 25 °C overcurrent trip level 10 V ⇔ 125 % I_C @ 25 °C current value > 0 ⇔ SKiiP is source current value < 0 ⇔ SKiiP is sink **SKiiP 3 with AlN ceramic substrate:** refer to corresponding datasheet
23	GND aux	reference for analog output signals
24	I analog OUT HB 2	as pin 22
25	GND aux	reference for analog output signals
26	I analog OUT HB 3	as pin 22

1) Open collector output, external pull up resistor necessary
2) „high“ (max) 12,3 V, „low“ (min) 4,6 V; SKiiP 3: 1 nF capacitance added signal to GND

PIN-array - brake chopper driver (used in SKiiP 2 type GDL)

X2:

Pin	signal	remark
1	shield	connected to GND (for usage of shielded cable)
2	CHOPPER ext. ON	LOW = IGBT ON „low“ (max) 5 V, I_{min} = 5 mA „high“ (min) 11,5 V propagation delay $t_{d(on)} \leq 20\ \mu s$ $t_{d(off)} \leq 25\ \mu s$
3	ERROR OUT[1)]	LOW = NO ERROR open collector Output; max. 30 V / 2,5 mA propagation delay$t_{PD(on)error} \leq 60\ \mu s$
4	RESET	LOW = RESET Reset-pulse-time $t_{PDRESET}$ > 300 ms connect this pin to open collector output **without** pull up resistor „low“ (max) 2 V, „high“ (min) 12 V
5	reserved	
6	+ 24 V_{DC} IN	don´t supply with 24 V, when using + 15 V_{DCIN} supply voltage monitoring threshold 15,6 V
7	+ 24 V_{DC} IN	
8	+ 15 V_{DC} IN	don´t supply with 15 V, when using + 24 V_{DCIN} supply voltage monitoring threshold 13 V
9	+ 15 V_{DC} IN	
10	GND	
11	GND	
12	reserved	
13	reserved	
14	reserved	

[1)] Open collector output, external pull up resistor necessary